POWER8 Processor Single Chip Module

Physical Outline Drawing

FC PLGA

Advance

March 25, 2014

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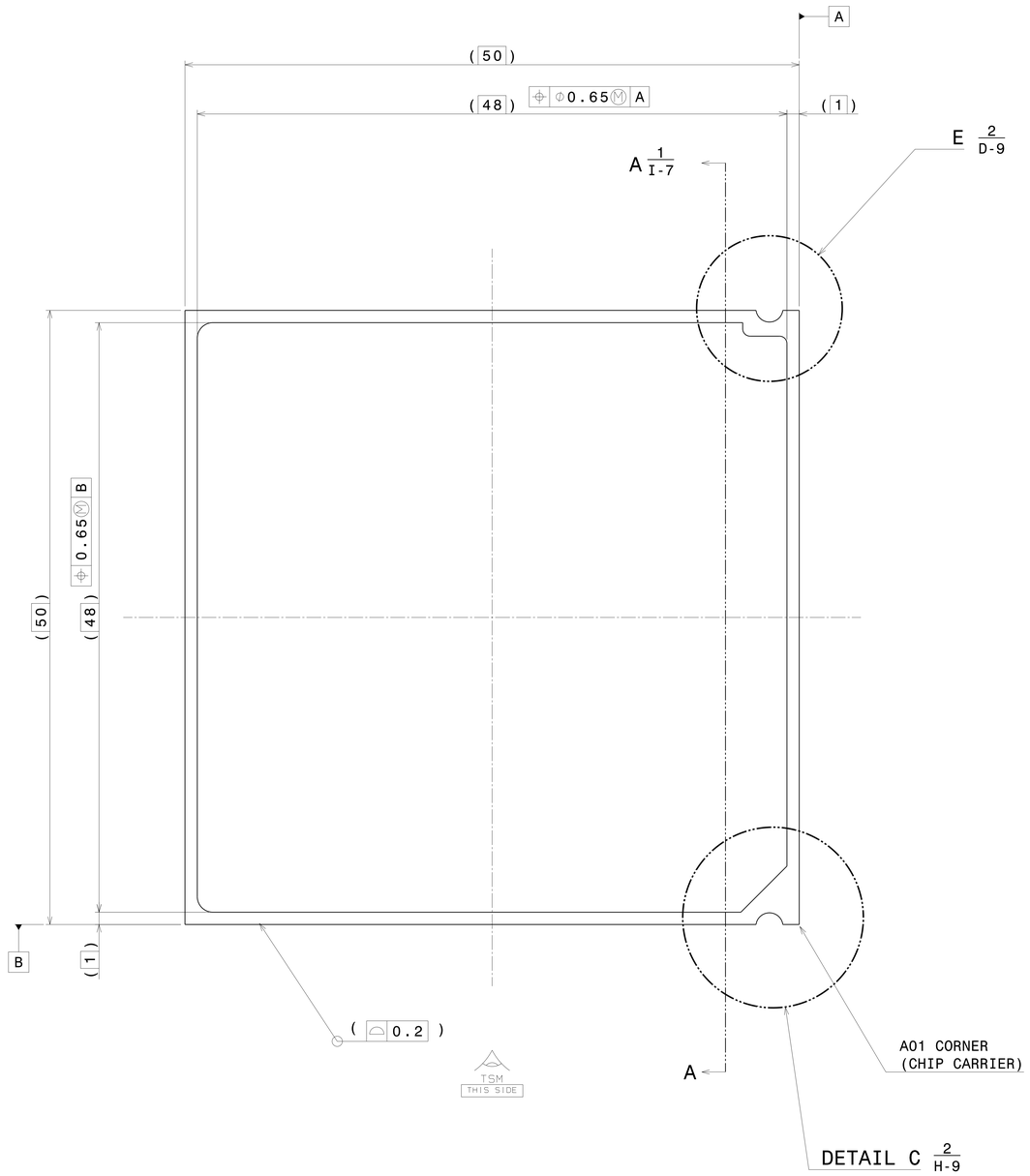
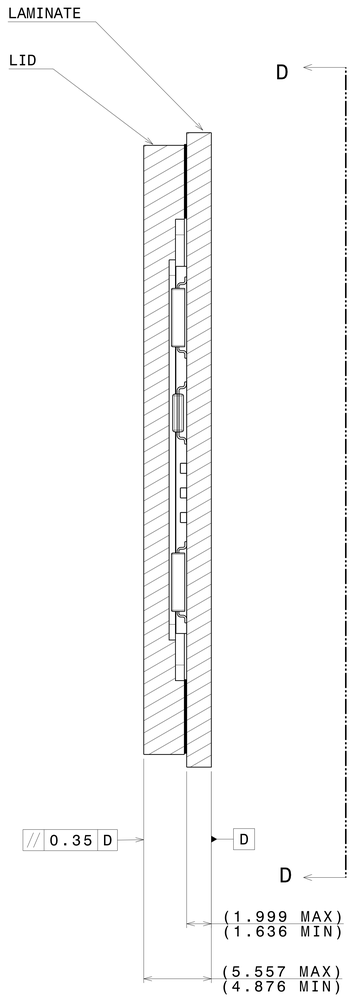
March 25, 2014





SECTION A-A 1/B-4

NOTES:

1. THIS PRODUCT IS ESD SENSITIVE. HANDLE IN ACCORDANCE WITH IBM PRODUCT DATA SHEET.
2. MODULE IS TO BE MARKED PER CUSTOMER APPLICATION.
3. DIMENSIONS WITH A MAX & MIN IN PARENTHESIS ARE APPROXIMATE, BASED ON MANUFACTURING PROCESS DEVIATION.
4. MODULE MUST CONFORM TO IBM ENG. SPEC. 00Y1911. IF APPLICABLE.
5. LGA LANDING PAD Cu THICKNESS 0.015. NiAu
   SURFACE FINISH: Ni≥0.003mm, 0.0005>Au>0.0003mm, NO SOLDER
   LGA LANDING PAD DIAMETERS 0.620/0.680.
   SOLDER RESIST MASK THICKNESS 0.015.
   SOLDER RESIST MASK OPENING DIAMETERS 0.720/0.780.
   SOLDER MASK MATERIAL MAY NOT TOUCH THE SIGNAL AND POWER LGA LANDING PADS.

SHEET 1 OF 2

SYM	DATE	EC NO.	SYM	DATE	EC NO.
REL	20140331	N93903			

MATERIAL/ SURFACE TREATMENT

SCALE: NONE

THIRD ANGLE PROJECTION

SI metric

TOLERANCE UNLESS NOTED

LINEAR ±	0.2
ANGLES ±	0° 30'
RADII UNLESS NOTED	

DESIGNER	KRL	20140325
APPROVED	LDS	20140325
CLASS	R0	20140331

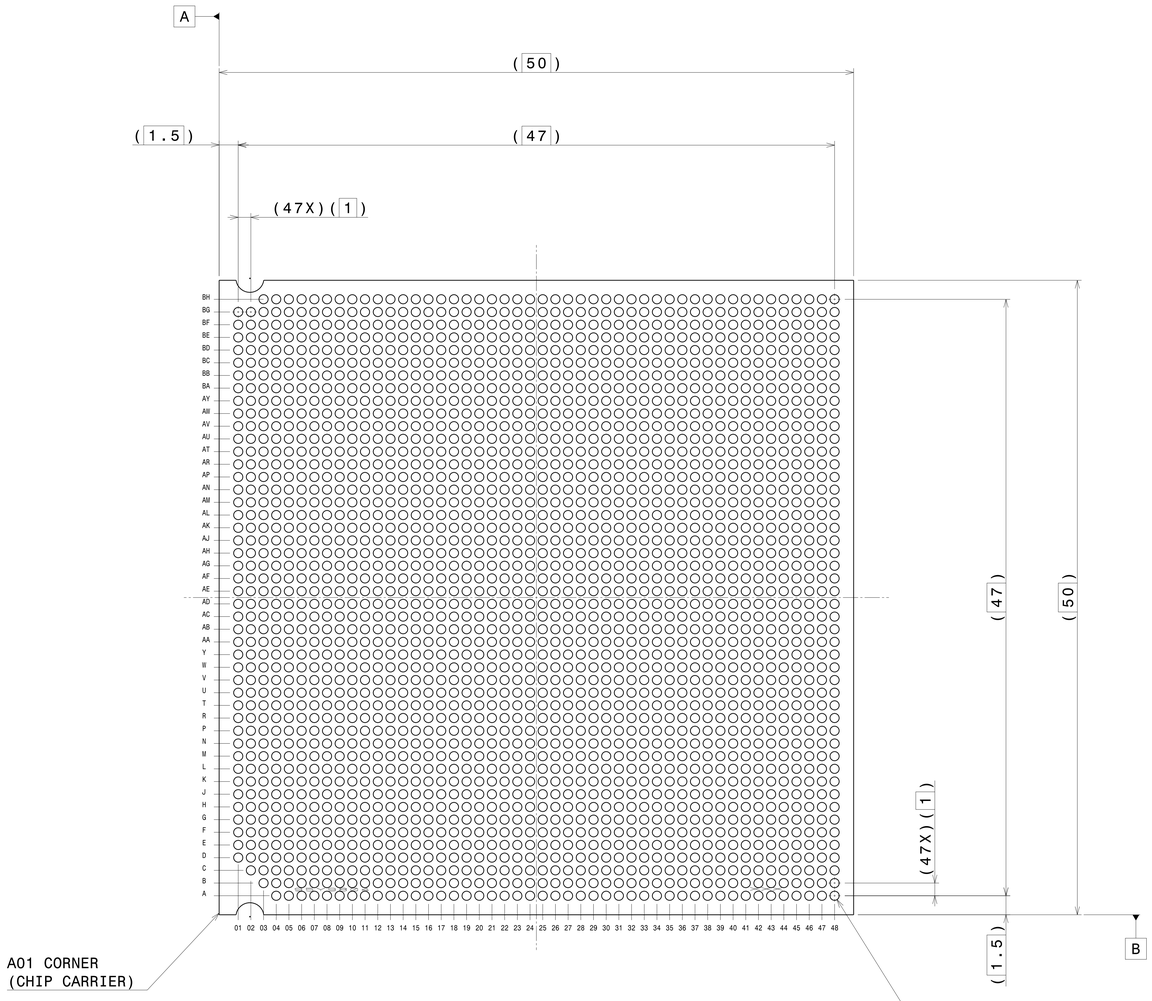
PART NO. 00Y1909

PREVIOUS PART NO.

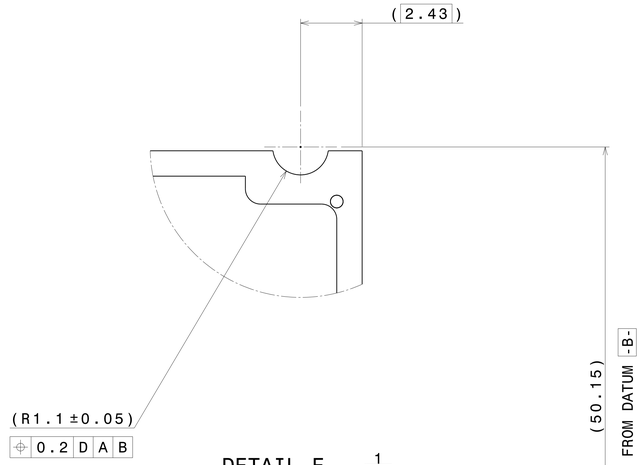
TITLE PHYSICAL OUTLINE, FC PLGA

POWER8 PROCESSOR SCM

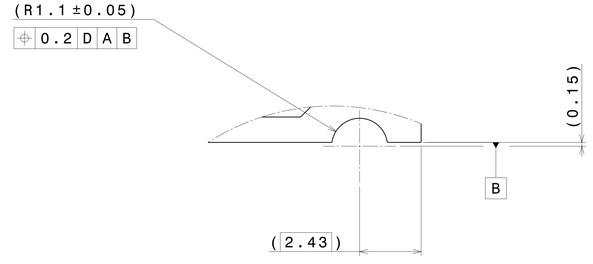
FORMAT CREATED IN CATIA ON V5R18
REF: IBMISO_Large_mm.xml DATED 20071002



SECTION VIEW D-D
SCALE: 6:1



DETAIL E 1/B-5
SCALE: ENLARGED



DETAIL C 1/H-5
SCALE: ENLARGED

BSM
THIS SIDE

SHEET 2 OF 2

SYM	DATE	EC NO.	SYM	DATE	EC NO.
REL	20140331	N93903			

MATERIAL/ SURFACE TREATMENT
SCALE: NONE
THIRD ANGLE PROJECTION
SI metric
TOLERANCE UNLESS NOTED
LINEAR ± 0.2
ANGLES ± 0° 30'
RADII UNLESS NOTED

DESIGNER	KRL	20140325
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