POWER8 Processor Single Chip Module

Packaging Applications Specification

FC PLGA

Advance

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1.0 Introduction

The technology described in this document addresses a module package that utilizes a C4 chip joined to an organic based, multilayer, laminate chip carrier. The module package consists of a coverplate which is adhesively attached to the chip and/or the substrate. Capacitors and/or other discrete devices may be attached to the laminate as well. The chip is underfilled to enhance package fatigue life. The coverplate is the interface for the customer's specific heat sink. The second level assembly connection for the module is a Land Grid Array (LGA).

1.1 Purpose

This specification describes the post module assembly and test final visual inspection requirements for the Flip-Chip/Plastic Land Grid Array (FC-PLGA) packages built using a qualified laminate chip carrier supplier. The inspection level described by this specification is post final test

This specification also defines to the module user:

1. Module shipping and handling procedures
2. Module visual requirements..
3. Second level assembly recommendations and product limitations

Flip Chip Plastic Land Grid Array (FC PLGA) module users must define and evaluate their assembly designs and processes to minimize assembled component damage.

1.2 Control

Packaging Product Engineering (PE), IBM Microelectronics Division, East Fishkill, NY USA, is responsible for the content and control of this specification.

1.3 Scope/Applicability

This specification describes to the module user the component requirements, limitations and card assembly/rework practices for lidded Flip Chip Plastic Land Grid Array (FC PLGA) modules. This specification is applicable where called for on an IBM Product or Technology Bill of Materials or Product Drawing. This specification is applicable to lead free FC PLGA.

IBM Module Physical Outline Drawings reference the following parameters, and shall be referred to as necessary:

- Package Type
- Package Physical Outline
- Module Body Size
- LGA Array
- LGA Pitch
- LGA Pad Size
- Solder Mask Opening

1.4 Precedence

In case of conflict between IBM requirements, this is the order of precedence, highest to lowest:
IBM Written Waivers/Off-Specifications
IBM Purchase Order
IBM Contract
IBM Part Number Drawing (or equivalent component description documentation)
Other IBM Specification that Document/Indicate a Higher Precedence
This Specification
Other IBM specifications Not Indicating Higher Precedence (e.g. Process, etc)
Referenced Industry Standards

2.0 Definitions

Active Area: The area of substrate containing metallized features.

AOQL: Average Outgoing Quality Limit. The AOQL is the poorest average quality level which the sample plan will deliver over a large stream of lots. The AOQL applies to sampling with rectification. That is, rejected lots are subject to 100% screening and, less importantly, to replacement or repair of defective items.

Blisters: Any raised area in the plating that has a voided interior.

BSM: Bottom Surface Metallurgy of the FC PLGA.

C4: Controlled Collapse Chip Connection (surface mount flip chip). .

Chip: missing material with defined edges

Coverplate: A protective lid attached to die with adhesive.

Delam: a delamination (separation) of layers

DI Water: De-Ionized Water

DNP: Distance from Neutral Point (center location of C4 flip chip or module BSM to outer most I/O connection)

ESD: Electrostatic Discharge

Foreign Material: Material either imbedded in laminate or on balls that cannot be brushed off or blown off as defined in the applicable manufacturing process specification.

I/O: Input/Output pad used for electrical connection/data transfer.

LGA Side: Side of the module which contacts the socket.

Laminate: Green colored plastic substrate material to which the die are attached.

Module Reuse: Removal of a module from a PCB assembly and attaching it to a different PCB assembly. **Note**: Module reuse is supported for FC PLGA modules, up to supported plug counts..

Pb Free: The content of lead is $\leq$1000 ppm by weight in each homogeneous material.

Pb Reduced: The content of lead is $\leq$1000 ppm by weight in each homogeneous material; except for lead present in flip chip bumps and the solder applied to connect the flip chip solder bumped chip or other components to its carrier.

Protective Coat: Soldermask or procoat covering conductive circuit features on the laminate.

PWB: Printed wiring board, also known as PCB, printed circuit board.

Scratch: a cut that displaces material

Second Level Assembly: All processes performed on a module or card during card assembly and test. For instance, vapor phase or IR joining, wave solder, module replacement and nearest neighbor rework.

Stain: Any discoloration or material foreign to the product which does not have measureable height. Presence and dimensions should be verifiable as viewed tops down at 10X/30X

Thermal Cycle: All processes that subject the module to an elevated and/or lowered temperature.

TSM: Top Surface Metallurgy of substrate

3.0 References

1. JEDEC Publication J-STD-033: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.
2. JEDEC Publication J-STD-020: Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.
3. ANSI/ESD S20.20 for the Development of an Electrostatic Discharge Control Program.
4. JEDEC Publication EIA625: Requirements for Handling Electrostatic-Discharge-Sensitive Devices.
5. JEDEC Standard, Test Method JESD22-A113-: Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing.
6. CO-029: JEDEC Registered Outline; Thin Matrix Tray for Shipping and Handling of Ball Grid Packages.
7. MIL-STD-81075, TYPE I: Requirements for flexibility, ESD protection, mechanical strength, and puncture resistance for protective moisture barrier bags.
8. MIL-D-3464, TYPE II: Requirements for desiccant material placed inside moisture barrier bags.
9. MIL-I-8835, MIL-P-116, Method II: Requirements for Humidity Indicator Card (HIC) placed inside a moisture barrier bag.
10. JEDEC Publication JEP113: Requirements for symbols and labels used for packaging of moisture sensitive devices.
11. IPC-D-275: Design Requirements of Printed Circuit Boards.
12. EIA/JESD22-B107, Marking Permanency.
13. JEDEC Publication 95 MS-034: Plastic BGA 1.0, 1.27, and 1.5mm pitch.

4.0 Module Inspection Requirements

4.1 General Inspection Requirements

4.1.1 Post module assembly and test, there shall be a visual inspection of the modules at 10X/verify at 30X magnification to guarantee 0.5% AOQL for all criteria in this ES, unless otherwise specified.

4.2 2nd Level Interconnect (LGA)

4.2.1 Defects such as residues, stains, contamination and/or solder residue less than 0.025 mm (0.001 in) from the metal of the LGA pads are not allowed.

4.2.2 A cumulative space free from residues, stains, contamination and/or solder residue, of 0.075 mm (0.003 in) is required between LGA pads. Foreign material or plating defects are allowed provided they do not reduce the cumulative free space requirement.

4.2.3 Maximum probe damage area of the IO pad combined with Voids/Foreign Material/Peeling/Blistering/Stains must not exceed 10% of I/O pad area. An edge defect which exposes the underlying laminate must not reduce the I/O pad diameter below the critical diameter size specified on the substrate drawing.

4.2.4 Dark yellow or gold stains on I/O pad area will be acceptable in the case where these stains are composed of Nickel oxide. Region of stain may extend onto the solder mask and the cumulative minimum spacing criteria between I/O pads doesn't have to be met. Probe marks must not be over 0.005 mm (.0002 inch) in height/depth. Probe marks or other mechanical damage are not allowed if it results in exposed nickel or copper.

4.2.5 No lifting of the BSM IO pad is allowed.

4.2.6 No exposed Cu or Ni is allowed on the I/O pads.

4.2.7 I/O Pad Depression Criteria: At least 50% of each I/O pad surface must be within 25 um (1 mil) in depth of the nearest neighboring I/O pads. The BSM surface must also meet the requirements of the applicable drawing

4.3 Laminate Criteria

4.3.1 Cracks or delamination in the laminate must not intrude by more than 0.25 mm (0.010 in) from the edge of the laminate.

4.3.2 Chipping starting at substrate edge that extend more than 0.51 mm (0.020 in) toward the center of the substrate are not allowed.

4.3.3 No exposed copper is allowed.

4.3.4 Delamination must not encompass conductors.

4.4 Module Inspection Criteria

4.4.1 Cracking, chipping or scratches in the protective coat starting at the substrate edge that extend more than 0.51 mm (0.020 in) from the edge of the substrate are not allowed.

4.4.2 Cracking scratches, or chipping in the protective coat, not starting at the substrate edge, that expose two conductive features are not allowed.

4.4.3 Defects such as voids, pinholes or discontinuities within the protective coat that expose two adjacent conductive features are not allowed.

4.4.4 A minimum region of 0.013 mm (0.0005 in) wide defect free protective coat must be present between conductors.

4.4.5 Voids/Foreign Material/Peeling/Blistering/Stains must not be over 0.05 mm (0.002 in) in height/depth.

4.4.6 Ink marks on the edges of the laminate are used for internal IBM tracking purposes and are allowed on the finished product.

4.4.7 Foreign material shall not protrude beyond outside edges of laminate or into laminate mousebites or alignment holes (interference with card socket alignment "keying" features identified in the drawings). Lid shall not interfere/overhang with laminate mousebites.

4.5 Ionic Contamination

4.5.1 Total ionic contamination (NaCl equivalent) on completed modules must not exceed 1.5 μg per cm^2 of total module surface area (top and bottom).

4.6 Coverplate

4.6.1 Visual inspection is to be performed at 1x.

4.6.2 No scratches or damage are allowed which expose base metal with the exception of plating contact points at coverplate edges.

4.6.3 No loose plating or foreign material is allowed.

4.6.4 Plating stains:

- Up to 5 stains per coverplate allowed with a maximum dimension of 0.5mm, each stain.

- Up to 4 stains per coverplate allowed with a maximum dimension of 2.5mm, each stain.
- Up to 2 stains per coverplate allowed with a maximum dimension of 4mm, each stain.

4.6.5 Other stains are allowed as long as they have no measurable height. They cannot obstruct marking readability. Second level processes may not cause permanent staining that impedes any aspect of module performance.

4.7 Marking Requirements

4.7.1 Marking is allowed on the exposed surface of the metal coverplate.

4.7.2 Ink should not exceed 30% cumulative of the coverplate area.

4.7.3 The text must be visible without magnification.

4.7.4 The marking format shall be per the applicable marking diagram as specified in the module bill of materials.

4.7.5 Marking permanency must meet the requirements of EIA/JESD22-B107.

4.7.6 Customer level marking as indicated on the marking drawing must be performed without ink cure.

5.0 Module Limitations and Handling

Modules shall be handled per JEDEC Publication J-STD-033: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices and EIA625; “Requirements for Handling Electrostatic-Discharge-Sensitive Devices”.

All packing and unpacking is to be done at a static control work station using procedures for handling described in the above cited documents. Prior to packing and unpacking an ESD sensitive item, neutralize charges on the static control container by placing the container on a static control table mat. Upon completion of the operation, the ESD sensitive items should immediately be placed back into the appropriate static shielding bag or static container.

5.1 ESD Handling Procedures

Refer to and maintain compliance with the ANSI/ESD S20.20 standard for the handling of ESD sensitive FC PLGA components.

5.2 Module Shipping and Storage

Modules will be packaged and shipped per JEDEC Publication J-STD-033: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices. IBM recommends that modules be handled at card assembly per J-STD-033.

FC PLGA product will be placed in JEDEC style trays (shall be in accordance with JEDEC Solid State Product Outline: CO-029 or CO-028) for shipment. All products will be oriented the same way in the trays. Product must be properly seated in the tray.

A maximum stack of ten (10) trays is permitted. An eleventh (empty) tray shall be placed on top of the completed stack of ten production trays. Stacked trays will be banded with nylon banding material and enclosed in a moisture barrier bags. Desiccant and a humidity indicator card (HIC) will be included in the MBB per J-STD-033.

- Moisture Barrier Bags: The moisture barrier shall have a maximum Water Vapor Transmission Rate (WVTR) of 0.005 g/100 in²/24 hours at room temperature after moisture/thermal aging per FED-STD-101C, Test Method 3030.1 and/or per JEDEC/IPC J-STD-033. Barrier material shall be non-corrosive and ESD protective. Minimum puncture resistance of 30 pounds is required. All cardboard shipping material must be external to the moisture barrier.

- Moisture Barrier Seal Integrity: A properly sealed vacuum bag conforms to the general shape of the internal contents, and has no rips, tears, punctures, or evidence of leakage.

- Packaging Water Vapor Transmission Rate Test (WVTR): This test is to determine the water vapor transmission rate of packaging materials. To conduct this test, see FED-STD-101 C Test Method 3030.1, Water Vapor Permeability Test of Packaging Materials".

The bag will be heat sealed and identified with a moisture sensitive identification label and a caution label. The modules will be packaged with the appropriate symbols and labels for moisture sensitive devices per EIA/JEDEC Publication EIA/JEP113. In addition to the above, each bag will have an attached label with the following information:

- Module part number
- Lot Number
- Quantity of modules
- Manufacturing date
- Manufacturing location
- JEDEC Moisture Sensitivity Classification and pertinent handling requirements

Sealed bags of product will be packaged in a cardboard box. The box will be labeled with the appropriate information per individual IBM/customer contracts.

The customer should notify IBM if the Humidity Indicator Card (HIC) is violated, the bag is punctured, or any other nonstandard/unacceptable condition exists.

5.3 Module Loading

0.040 kgf (0.39 N, 0.0876 lbf.) nominal, +/- 15% per LGA pad represents typical loading used during IBM module testing. In IBM's testing, care was taken to uniformly support all the LGA's. The load was applied with a rigid, flat surface which was parallel to, and covered the entire coverplate surface. These guidelines are based on IBM's socket apparatus. Due to the large number of socket designs available, the user should verify that the socket chosen doesn't damage the module.

Lid adhesive materials are susceptible to handling damage when exposed to temperatures above 150°C. It is intended that no force be applied to FC PLGA components at temperatures above 150°C.

5.4 FC PLGA PCB Recommended Design Guidelines

Consideration of the following design guidelines is recommended to promote robust FC PLGA module to printed circuit board assembly:

5.4.1 Printed circuit boards should meet design requirements in IPC-2221 and IPC-2222.
5.4.2 Printed circuit boards should be designed with symmetrical card cross section.
5.4.3 Consider form factor of the cards - large thin cards are more likely to warp during processing and may require fixtures.
5.4.4 Sockets must meet flatness and coplanarity (<0.050 mm) requirements at the time of module insertion.

5.5 FC PLGA Placement & Socketing

5.5.1 Manual placement and/or manual repositioning of FC PLGA modules is acceptable.

5.5.2 FC PLGA modules may be re-socketed a maximum of 9 times (10 total plug cycles).

5.5.3 IBM used a nominal socketing force of 40 (0.39 N) grams per LGA pad during the build of FC PLGA modules used in the module package qualification cells.

5.5.4 In extreme cases of handling and process induced card bending, torquing or impact shock, assembled component damage can occur. The assembled component and/or component to card interconnection can be affected.

5.5.5 During In Circuit Test (ICT):

- Minimize electrical probe loading and bending stress. Use uniform probe and support placement, avoid support placements located within about 10mm of component corners and use support placements located near all four of the component mid-sides).
- Minimize probe placements behind LGA components. Allowable probe count will depend on board design, support fixture design, and probe loading.
- Minimize the number of ICT passes.

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