POWER8 Memory Buffer

Datasheet

Advance

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IBM Systems and Technology Group
2070 Route 52, Bldg. 330
Hopewell Junction, NY 12533-6351

The IBM home page can be found at **ibm.com®**.

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Revision Log

Version	Revision Date	Pages	Description
1.1	22 April 2014	–	First public release.
1.0	31 January 2014	–	Initial release.

About this Datasheet

This book is a technical reference for the IBM® POWER8™ Memory Buffer. It contains detailed technical information and specifications including interface definitions, input/output (I/O) signals, specifications, timing specifications, and other related information.

Throughout this document, the term “memory buffer” refers to the POWER8 Memory Buffer.

To obtain the most current version of this document, contact your IBM technical representative or visit the IBM Customer Connect website.

Who Should Use this Book

This book is intended for use by hardware and software designers when developing products containing the POWER8 Memory Buffer.

Conventions

Notation for bit encoding is as follows:

- Hexadecimal values are preceded by an x and enclosed in single quotation marks. For example: x‘0A00’.
- Binary values in sentences appear in single quotation marks. For example: ‘1010’.

1. Overview

1.1 Functional Description

The IBM POWER8 Memory Buffer is a memory buffer chip that supports multiple system configurations. The POWER8 Memory Buffer uses a high-speed differential interface to communicate with a processor chip using a memory-agnostic protocol. The memory controller and associated memory interface maintenance and calibration functions are initiated and contained within the memory buffer chip. It also contains a 16 MB on-board cache to support prefetching and improve system performance.

1.1.1 Technology

The POWER8 Memory Buffer is a synchronous memory interface chip, manufactured using the 22 nm CMOS 14S technology with 15 metal layers. It has four memory ports and 16 MB of cache. A high-speed differential memory interface connects the memory buffer to the processor chip. The memory buffer supports DDR3 DRAM technologies.

1.2 Features

Table 1-1 lists significant features of the memory buffer.

Table 1-1. Feature Summary (Page 1 of 2)

Feature Type	Description
Basic features	• A single differential memory interface running at 9.6 Gbps • Four DDR3 DRAM command and address ports • Four 8-byte DDR3 DRAM data ports with a 9th byte for ECC • 32 addressable ranks (16 per port pair) • 16 clock enables (CKEs) and on-die termination (ODT) (four per port) • 16 differential memory clock pairs (four per port) • 16 MB 16-way associative cache employing eDRAM
Operational modes	• 128-byte (BL8) cache-line read and write operations • Partial 128-byte cache-line write operations (read-modify-write) • Return to high-impedance (Hi-Z) state on command/address ports • Cache disable • 2N addressing mode (2 bits per cycle)
Memory channel	• 9.6 Gbps differential ended unidirectional signals • Downstream link: 14+2+1+1 (data, spares, calibration, clock) • Upstream link: 21+2+1+1 (data, spares, calibration, clock) • Spare lane signaling enables dynamic link training and repair

Table 1-1. Feature Summary (Page 2 of 2)

Feature Type	Description
Power saving	• DRAM power down • Advanced run-time power management policies • Support for fast and slow exit power down of DRAMs • Aggressive dynamic clock gating
Manufacturing, test, and bringup	• Maintenance engine for initial program load (IPL) memory diagnostics • Memory card built-in self test (MCBIST) • Hard and soft error injection stations for DDR data and command/address ports • Memory channel link self test diagnostics • IEEE 1149.6 boundary scan wire test capability • Source selectable trace array • Two scope trigger pins with configurable events and measurement sources • Digital temperature and voltage sensor (TVSENSE) • On-product clock generation logic built-in self test (LBIST) • Array built-in self test (ABIST) for eDRAMs and SRAMs with corresponding eFUSE repair structure • Rank Status Register for tracking reset, power down, and self refresh state of DRAM devices • Fully-accessible configuration registers through Flexible Service Interface (FSI) and IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture (JTAG) scan communications (SCOM), millicode, and level-sensitive scan design (LSSD) scanning • Performance Monitor interface for frequency measurements of critical events, and measurements of power events • Electronic chip identification (ECID) for manufacturing part tracking • Debug bus interface
Reliability, availability, and serviceability (RAS)	• Service processor slave interface powered by V_{SB} standby voltage employing FSI protocol • Hierarchical Fault Isolation Register (FIR) error detection structure with configurable severity masks • Chip kill support for x4 and x8 DRAM devices • Memory scrubbing • Bidirectional fault signal to respond to, or drive out, checkstop requests • Attention indicator that can be polled by the service interface • Memory channel protected by strong cyclic redundancy check (CRC) with automatic retransmission (replay) of packet errors • Configurable fast clock stop on fault • Dynamic lane sparing on memory channel to repair faulty lanes concurrently during mainline operation • All critical data flow and control elements are protected by either ECC, parity, or a soft error (SER) hardened latch

1.3 General Parameters

Table 1-2. Parameter Summary

Feature Type	Description
Technology	• 22 nm CMOS SOI (14S) • Reliability grade 3 (72 KPOH, 2555 on/off cycles) • Chip image: 9.262 mm × 11.136 mm (103.14 sq. mm) • C4 pitch: 185.6 µm X, 148.48/185.6 µm Y (variable) • Packages: – 4 port, 27.5 mm × 42 mm 3-2-3 FC-PBGA with 1.0 mm interstitial pitch – 3240 controlled collapse chip connections (C4s) with 867 signal I/Os
Power planes (at module)	• V_{DD} core voltage ..... 0.969 V • V_{CS} eDRAM supply ..... 1.090 V • V_{IO} differential memory interface (DMI) and pervasive I/O ..... 1.127 V • V_{DDR} DDR PHY DDR3 ..... 1.35 V • AV_{DD} analog supply ..... 1.502 V • V_{SB} service interface ..... 1.208 V
Operational maximum frequency targets	Memory channel..... 9.6 Gbps DDR3 ..... 1600 Mbps

2. Electrical Characteristics

2.1 Power Planes

The following externally referenced power planes are available on the memory buffer:

- V_{DD} core voltage .....0.969 V
- V_{CS} eDRAM supply .....1.090 V
- V_{IO} differential memory interface (DMI) and pervasive I/O.....1.127 V
- V_{DDR} DDR PHY
  DDR3 .....1.35 V
- AV_{DD} analog supply.....1.502 V
- V_{SB} service interface .....1.208 V

2.2 Clock Domains and Operational Frequencies

The memory buffer supports the following operational domains:

- 8.0 or 9.6 Gbps DMI link.
- Synchronous memory channel interface with fixed 4:1 ratio to the DMI link
- Asynchronous memory controller operating at the DDR frequency of the currently installed DRAMs. The memory buffer supports the following DRAM technologies and data rates:
  - DDR3 1.35 V running at 1333 and 1600 Mbps.
- Memory clock domain for supplying single-ended reference clocks to the embedded DDR PHY PLLs. This domain runs at exactly half of the frequency of the installed DRAM data rate. (See above for supported DDR speeds).
- 166 MHz service interface domain.
- Two external reference clocks driving two discrete PLLs.
  - One 133 MHz reference clock PLL drives the 2.4 GHz synchronous domain.
  - Another 133 MHz reference clock PLL drives the asynchronous memory domain operating at the DDR frequency.

2.3 Required Operating Conditions

Table 2-1. Universal Application Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
DDR I/O Voltage	V_{DDR}	1.28	1.35	1.42	V	1
DMI and Pervasive I/O Voltage	V_{IO}	1.017	1.127	1.184	V	1
CFAM Standby Voltage	V_{SB}	1.148	1.208	1.268	V	1
Analog Voltage	AV_{DD}	1.427	1.502	1.577	V	1

1. At the module pin.
2. Maximum junction temperature is supported under all environmental conditions
3. Based on the formula $V_{CS} = 0.44 + (0.66 \times V_{DD})$.

Table 2-1. Universal Application Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
L4 eDRAM Voltage	V_{CS}	1.036	1.090	1.145	V	1, 3
Core Voltage	V_{DD}	0.921	0.969	1.017	V	1
Junction Temperature	T_j	0	75	95	C	2

1. At the module pin.
2. Maximum junction temperature is supported under all environmental conditions
3. Based on the formula $V_{CS} = 0.44 + (0.66 \times V_{DD})$.

Table 2-2. Grade 3 Application Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Machine Life	-	8	-	-	Years	
Machine Life	-	72	-	-	KPOH	
On / Off Cycles	-	-	-	2555	-	
Mini Cycles per Day	-	-	-	25	-	
Nominal Tj	Tjnom	-	-	95	C	1

1. Maximum nominal temperature is used for reliability calculations.

2.4 Electrostatic Discharge Considerations

This product is electrostatic discharge (ESD) sensitive. An appropriate ESD handling procedure must be implemented and maintained by facilities handling this component. Handle according to the ANSI/ESD S20.20 or IEC 61340-5-1. Packaging of this product in an ESD safe container should be according to ANSI/ESD S541 or IEC 61340-5-3.

3. I/O Characteristics

3.1 Functional I/Os

The following notes pertain to the functional I/Os:

- On the D3PHY interface, ERRN, EVENTN, and RESETN are not part of the high-speed PHY interface. They are regular tristate drivers and not part of BIST and are used to control D3PHY operation during test. They are not affected by the IO_TP_SHARED_DRIVERS function.
- Internal tie resistors are all 10 K unless otherwise indicated.

3.2 Special Test Pins

The following test pins are only used or modified on the POWER8 Memory Buffer (not the POWER8 Processor).

Figure 3-1. Special Test Pins

Name	Conditions	Function
IO_TP_SHARED_DRIVERS	CE0_TE = 0	No effect.
	CE0_TE = 1	0: Normal test mode. 1: Locally removes the TE = 1 condition to the I/O on the ADR DPHY pins. Allows them to be characterized during manufacturing test. The chip must be in a functional state when doing this (for example, the clocks are running). **Note:** This only affects ADR macros. It does not affect the IOG transceivers used on the PHY interface (ERRN, EVENTN, RESETN).
IO_TP_TEST_MACROTEST_DC	CE0_TE = 0	No effect.
	CE0_TE = 1	0: Macro test disabled. 1: Enables ASIC macrotest modes. Also enables the D3PHY PLLs to drive TEST and LOCK out to shared test I/O.
IO_TP_MC_DC	CE0_TE = 0	No effect.
	CE0_TE = 1	Works in conjunction with MacroTest mode.
IO_TP_TEST_DLT_DC	CE0_TE = 0	No effect.
	CE0_TE = 1	Dynamic Leakage Test. A special version of IO_TP_IDDQ_DC used during burn-in only
IO_TP_FORCETOKNOWN_DC	CE0_TE = 0	No effect.
	CE0_TE = 1	1: Forces analog circuitry in the D3PHY to a known state.
IO_DDR_JTAGSHIFTDR IO_DDR_JTAGTDI DDR[0123]_IO_JTAGTD0 IO_DDR_JTAGCLOCKDR IO_DDR_JTAGINSTRDCD IO_DDR_JTAGUPDATEDR	CE0_TE = 1 and MACROTEST = 1	Special JTAG interface for accessing and controlling the D3PHY during macrotest mode.
IO_TP_TEST_SCAN_DIAG_DC	CE0_TE = 1	On the memory buffer, this is derived by io_tp_test_scan_diag_array_set_dc and not(io_tp_test_scan_out_en_dc)
IO_TP_TEST_ARRAY_SET_VBL_TO_VDD_DC	CE0_TE = 1	On the memory buffer, this is derived by io_tp_test_scan_diag_array_set_dc and io_tp_test_scan_out_en_dc

3.3 Power Pins and Voltage Monitors

Table 3-1. Power Pins and Voltage Monitors

Chip I/O	Dir	Description	Module Rail	System Rail	Nominal Voltage (Volts)	Max Freq (MHz)	Quantity
AGND_D0R	I	Analog ground DMI RX PLL	AGND	GND	0	N/A	1
AGND_D0T	I	Analog ground DMI TX PLL	AGND	GND	0	N/A	1
AGND_MEM	I	Analog ground PLLMEM	AGND	GND	0	N/A	1
AVDD_D0R	I	Analog voltage DMI RX PLL	AVDD	VDDA	1.5	9600	1
AVDD_D0T	I	Analog voltage DMI TX PLL	AVDD	VDDA	1.5	9600	1
AVDD_MEM	I	Analog voltage PLLMEM	AVDD	VDDA	1.5	9600	1
AVDDR_MA[012345][A]	I	Analog voltage, DPHY PLL, MA Port (one pin per PLL)	VDDR	VMEM	1.35	966	12
AVDDR_MB[012345][A]	I	Analog voltage, DPHY PLL, MB Port (one pin per PLL)	VDDR	VMEM	1.35	966	12
AVDDR_MC[012345][A]	I	Analog voltage, DPHY PLL, MC Port (one pin per PLL)	VDDR	VMEM	1.35	966	12
AVDDR_MD[012345][A]	I	Analog voltage, DPHY PLL, MD Port (one pin per PLL)	VDDR	VMEM	1.35	966	12
GND	I	Ground	GND	GND	0	N/A	1141
VCS	I	EDRAM voltage	VCS	VCSC	1.034	3000	190
VDD	I	Memory buffer core voltage	VDD	VDDC	0.90	2400	568
VDDR	I	DDR I/O voltage (DVDD on D3Phy core)	VDDR	VMEM	1.35	1866	374
VIO	I	DMI I/O voltage	VIO	VIO	1.1	4800	28
VSB	I	Voltage standby for CFAM voltage island	VSB	VDDSTBY	1.2	166	18
REFAVDD[0,1,2]	I	Analog Reference Voltage. For DPHY port A	VDDR	VMEM	1.35	N/A	3
REFAVDD[3,4,5]	I	Analog Reference Voltage. For DPHY port B	VDDR	VMEM	1.35	N/A	3
REFAVDD[6,7,8]	I	Analog Reference Voltage. For DPHY port C	VDDR	VMEM	1.35	N/A	3
REFAVDD[9, 10, 11]	I	Analog Reference Voltage. For DPHY port D	VDDR	VMEM	1.35	N/A	3
VMON_GND	O	Voltage Monitor Signals. (Ground Plane)					1
VMON_VCS	O	Voltage Monitor Signals. (EDRAM voltage)					1
VMON_VDD	O	Voltage Monitor Signals. (General-purpose digital voltage)					1
VMON_VDDR	O	Voltage Monitor Signals. (DDR I/O voltage)					1
VMON_VIO	O	Voltage Monitor Signals. (DMI I/O voltage)					1
VMON_VPP0	O	Voltage Monitor Signals. (TEST I/O) (EDRAM Charge Pumps *not* card VPP)					1
VMON_VPP1	O	Voltage Monitor Signals. (TEST I/O) (EDRAM Charge Pumps *not* card VPP)					1

Table 3-1. Power Pins and Voltage Monitors

Chip I/O	Dir	Description	Module Rail	System Rail	Nominal Voltage (Volts)	Max Freq (MHz)	Quan-tity
VMON_VSB	O	Voltage Monitor Signals. (FSI standby voltage)					1
VMON_VWL0	O	Voltage Monitor Signals. (TEST I/O) (EDRAM word line regulator)					1
VMON_VWL1	O	Voltage Monitor Signals. (TEST I/O) (EDRAM word line regulator)					1

4. Signal Descriptions

4.1 Signal I/Os

Table 4-1. Signal I/Os (Page 1 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
FM041	agnd_d0r	AGND	AG25
GU041	agnd_d0t	AGND	AG25
GB056	agnd_mem	AGND	AG25
FG041	avdd_d0r	AVDD	AH26
HB041	avdd_d0t	AVDD	AH26
GG056	avdd_mem	AVDD	AH26
PE021	avddr_ma0a	VDDR	See *Section 4.2 Power Rails* on page 44 for the BGA list.
PE026	avddr_ma0a	VDDR	
RA081	avddr_ma1a	VDDR	
RE081	avddr_ma1a	VDDR	
NA081	avddr_ma2a	VDDR	
NE081	avddr_ma2a	VDDR	
MA021	avddr_ma3a	VDDR	
LU021	avddr_ma3a	VDDR	
RA121	avddr_ma4a	VDDR	
RE121	avddr_ma4a	VDDR	
NA121	avddr_ma5a	VDDR	
NE121	avddr_ma5a	VDDR	
PE221	avddr_mb0a	VDDR	
PE216	avddr_mb0a	VDDR	
RA161	avddr_mb1a	VDDR	
RE161	avddr_mb1a	VDDR	
NA161	avddr_mb2a	VDDR	
NE161	avddr_mb2a	VDDR	
MA221	avddr_mb3a	VDDR	
LU221	avddr_mb3a	VDDR	

Table 4-1. Signal I/Os (Page 2 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
KJ221	avddr_mb4a	VDDR	See *Section 4.2 Power Rails* on page 44 for BGA list.
KN221	avddr_mb4a	VDDR	
JA221	avddr_mb5a	VDDR	
JE221	avddr_mb5a	VDDR	
BE216	avddr_mc0a	VDDR	
BE221	avddr_mc0a	VDDR	
AJ161	avddr_mc1a	VDDR	
AE161	avddr_mc1a	VDDR	
CE161	avddr_mc2a	VDDR	
CJ161	avddr_mc2a	VDDR	
DJ221	avddr_mc3a	VDDR	
DN221	avddr_mc3a	VDDR	
EU221	avddr_mc4a	VDDR	
FA221	avddr_mc4a	VDDR	
GE221	avddr_mc5a	VDDR	
GJ221	avddr_mc5a	VDDR	
BE021	avddr_md0a	VDDR	
BE026	avddr_md0a	VDDR	
AJ081	avddr_md1a	VDDR	
AE081	avddr_md1a	VDDR	
CE081	avddr_md2a	VDDR	
CJ081	avddr_md2a	VDDR	
DJ021	avddr_md3a	VDDR	
DN021	avddr_md3a	VDDR	
AJ121	avddr_md4a	VDDR	
AE121	avddr_md4a	VDDR	
CJ121	avddr_md5a	VDDR	
CE121	avddr_md5a	VDDR	
HJ216	c4_cal_ddr_g	cal_ddr_g	AE21
HN216	c4_cal_ddr_r	cal_ddr_r	AF18
HM046	c4_cal_dmitx_g	cal_dmitx_g	AF30
HU046	c4_cal_dmitx_r	cal_dmitx_r	AE29
LG001	c4_ce0_te	ce0_te	U41
LG006	c4_cfam_reset_b	cfam_reset_b	R43
GG061	c4_ddr_refck_n	ddr_refck_n	AJ31
GM061	c4_ddr_refck_p	ddr_refck_p	AK32
GM056	c4_ddrpll_anl_tst	ddrpll_anl_tst	AG29

Table 4-1. Signal I/Os (Page 3 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
GB061	c4_ddrpll_dgt_tst	ddrpll_dgt_tst	AH32
GU216	c4_diff_probe_n<0>	diff_probe_n<0>	AG19
GU226	c4_diff_probe_n<1>	diff_probe_n<1>	AG17
HA216	c4_diff_probe_p<0>	diff_probe_p<0>	AH20
HA226	c4_diff_probe_p<1>	diff_probe_p<1>	AH18
KG011	c4_dio<0>	dio<0>	AC31
KG016	c4_dio<1>	dio<1>	AB26
GU046	c4_dmi_refck_n	dmi_refck_n	AE33
HB046	c4_dmi_refck_p	dmi_refck_p	AF32
FB041	c4_dmids_ck_n	dmids_ck_n	AP42
EU041	c4_dmids_ck_p	dmids_ck_p	AN41
FB046	c4_dmids_minikerf_n	dmids_minikerf_n	AN35
EU046	c4_dmids_minikerf_p	dmids_minikerf_p	AM34
FB001	c4_dmids_n<0>	dmids_n<0>	AT38
FB006	c4_dmids_n<1>	dmids_n<1>	AN37
FU016	c4_dmids_n<10>	dmids_n<10>	AN45
FU031	c4_dmids_n<11>	dmids_n<11>	AR47
FU021	c4_dmids_n<12>	dmids_n<12>	AM44
FU026	c4_dmids_n<13>	dmids_n<13>	AL43
FU011	c4_dmids_n<14>	dmids_n<14>	AM46
FU036	c4_dmids_n<15>	dmids_n<15>	AM40
FU041	c4_dmids_n<16>	dmids_n<16>	AM38
FB031	c4_dmids_n<2>	dmids_n<2>	AT40
FB026	c4_dmids_n<3>	dmids_n<3>	AN39
FB021	c4_dmids_n<4>	dmids_n<4>	AT42
FB016	c4_dmids_n<5>	dmids_n<5>	AP44
FB011	c4_dmids_n<6>	dmids_n<6>	AT44
FB036	c4_dmids_n<7>	dmids_n<7>	AV46
FU001	c4_dmids_n<8>	dmids_n<8>	BB46
FU006	c4_dmids_n<9>	dmids_n<9>	AY46
EU001	c4_dmids_p<0>	dmids_p<0>	AU37
EU006	c4_dmids_p<1>	dmids_p<1>	AP38
GB016	c4_dmids_p<10>	dmids_p<10>	AP46
GB031	c4_dmids_p<11>	dmids_p<11>	AT46
GB021	c4_dmids_p<12>	dmids_p<12>	AL45
GB026	c4_dmids_p<13>	dmids_p<13>	AM42
GB011	c4_dmids_p<14>	dmids_p<14>	AL47

Table 4-1. Signal I/Os (Page 4 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
GB036	c4_dmids_p<15>	dmids_p<15>	AL41
GB041	c4_dmids_p<16>	dmids_p<16>	AL39
EU031	c4_dmids_p<2>	dmids_p<2>	AU39
EU026	c4_dmids_p<3>	dmids_p<3>	AP40
EU021	c4_dmids_p<4>	dmids_p<4>	AU41
EU016	c4_dmids_p<5>	dmids_p<5>	AN43
EU011	c4_dmids_p<6>	dmids_p<6>	AU43
EU036	c4_dmids_p<7>	dmids_p<7>	AU45
GB001	c4_dmids_p<8>	dmids_p<8>	BC47
GB006	c4_dmids_p<9>	dmids_p<9>	AW47
GU036	c4_dmipll_anl_tst	dmipll_anl_tst	BE47
GU031	c4_dmipll_hfc_n	dmipll_hfc_n	AK34
HB031	c4_dmipll_hfc_p	dmipll_hfc_p	AH34
HU021	c4_dmius_ck_n	dmius_ck_n	AC41
HM021	c4_dmius_ck_p	dmius_ck_p	AB42
GU001	c4_dmius_n<0>	dmius_n<0>	AH36
GU006	c4_dmius_n<1>	dmius_n<1>	AF38
HU026	c4_dmius_n<10>	dmius_n<10>	AG47
HU031	c4_dmius_n<11>	dmius_n<11>	AF36
HU036	c4_dmius_n<12>	dmius_n<12>	AB46
HU041	c4_dmius_n<13>	dmius_n<13>	Y46
JG001	c4_dmius_n<14>	dmius_n<14>	AC43
JG006	c4_dmius_n<15>	dmius_n<15>	V46
JG011	c4_dmius_n<16>	dmius_n<16>	U47
JG016	c4_dmius_n<17>	dmius_n<17>	AC39
JG021	c4_dmius_n<18>	dmius_n<18>	Y44
JG026	c4_dmius_n<19>	dmius_n<19>	Y42
GU011	c4_dmius_n<2>	dmius_n<2>	AH38
JG031	c4_dmius_n<20>	dmius_n<20>	W39
JG036	c4_dmius_n<21>	dmius_n<21>	W37
JG041	c4_dmius_n<22>	dmius_n<22>	AB36
JG046	c4_dmius_n<23>	dmius_n<23>	AB38
GU021	c4_dmius_n<3>	dmius_n<3>	AF40
GU016	c4_dmius_n<4>	dmius_n<4>	AH40
GU026	c4_dmius_n<5>	dmius_n<5>	AE41
HU001	c4_dmius_n<6>	dmius_n<6>	AG43
HU006	c4_dmius_n<7>	dmius_n<7>	AE43

Table 4-1. Signal I/Os (Page 5 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
HU011	c4_dmius_n<8>	dmius_n<8>	AG45
HU016	c4_dmius_n<9>	dmius_n<9>	AE45
HB001	c4_dmius_p<0>	dmius_p<0>	AG37
HB006	c4_dmius_p<1>	dmius_p<1>	AE37
HM026	c4_dmius_p<10>	dmius_p<10>	AH46
HM031	c4_dmius_p<11>	dmius_p<11>	AE35
HM036	c4_dmius_p<12>	dmius_p<12>	AC45
HM041	c4_dmius_p<13>	dmius_p<13>	AA47
JM001	c4_dmius_p<14>	dmius_p<14>	AB44
JM006	c4_dmius_p<15>	dmius_p<15>	W45
JM011	c4_dmius_p<16>	dmius_p<16>	T46
JM016	c4_dmius_p<17>	dmius_p<17>	AB40
JM021	c4_dmius_p<18>	dmius_p<18>	W43
JM026	c4_dmius_p<19>	dmius_p<19>	W41
HB011	c4_dmius_p<2>	dmius_p<2>	AG39
JM031	c4_dmius_p<20>	dmius_p<20>	Y40
JM036	c4_dmius_p<21>	dmius_p<21>	Y38
JM041	c4_dmius_p<22>	dmius_p<22>	AC35
JM046	c4_dmius_p<23>	dmius_p<23>	AC37
HB021	c4_dmius_p<3>	dmius_p<3>	AE39
HB016	c4_dmius_p<4>	dmius_p<4>	AG41
HB026	c4_dmius_p<5>	dmius_p<5>	AF42
HM001	c4_dmius_p<6>	dmius_p<6>	AH42
HM006	c4_dmius_p<7>	dmius_p<7>	AF44
HM011	c4_dmius_p<8>	dmius_p<8>	AH44
HM016	c4_dmius_p<9>	dmius_p<9>	AF46
HE206	c4_fault_n	fault_n	AG21
LG011	c4_fsi_sel_b	fsi_sel_b	R47
KU001	c4_fsic0	fsic0	T44
KM001	c4_fsic1	fsic1	N47
KU006	c4_fsid0	fsid0	T42
KM006	c4_fsid1	fsid1	P44
KU041	c4_fsource	fsource	AA27
KM016	c4_iot_card_test_bsc	iot_card_test_bsc	AB34
PJ056	c4_ma_atst<0>	ma_atst<0>	J35
NA016	c4_ma_atst<1>	ma_atst<1>	J47
PE016	c4_ma_cmd_a<0>	ma_cmd_a<0>	F46

Table 4-1. Signal I/Os (Page 6 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
NU031	c4_ma_cmd_a<1>	ma_cmd_a<1>	E45
RE006	c4_ma_cmd_a<10>	ma_cmd_a<10>	M40
RE041	c4_ma_cmd_a<11>	ma_cmd_a<11>	E43
PE006	c4_ma_cmd_a<12>	ma_cmd_a<12>	H44
PE041	c4_ma_cmd_a<13>	ma_cmd_a<13>	B42
NJ041	c4_ma_cmd_a<14>	ma_cmd_a<14>	D42
PA016	c4_ma_cmd_a<15>	ma_cmd_a<15>	L37
NU036	c4_ma_cmd_a<2>	ma_cmd_a<2>	D44
PN031	c4_ma_cmd_a<3>	ma_cmd_a<3>	G43
NJ031	c4_ma_cmd_a<4>	ma_cmd_a<4>	E47
PJ031	c4_ma_cmd_a<5>	ma_cmd_a<5>	C47
PA031	c4_ma_cmd_a<6>	ma_cmd_a<6>	F42
RA036	c4_ma_cmd_a<7>	ma_cmd_a<7>	B44
RE031	c4_ma_cmd_a<8>	ma_cmd_a<8>	G41
RA031	c4_ma_cmd_a<9>	ma_cmd_a<9>	C45
RE036	c4_ma_cmd_actn	ma_cmd_actn	K34
PE031	c4_ma_cmd_ba<0>	ma_cmd_ba<0>	K36
PJ036	c4_ma_cmd_ba<1>	ma_cmd_ba<1>	G37
RA041	c4_ma_cmd_ba<2>	ma_cmd_ba<2>	H36
PN036	c4_ma_cmd_casn	ma_cmd_casn	M32
RJ056	c4_ma_cmd_errn	ma_cmd_errn	B46
RE056	c4_ma_cmd_eventn	ma_cmd_eventn	H38
NU016	c4_ma_cmd_par	ma_cmd_par	K38
NE031	c4_ma_cmd_rasn	ma_cmd_rasn	R35
PN056	c4_ma_cmd_resetn	ma_cmd_resetn	C41
PJ041	c4_ma_cmd_wen	ma_cmd_wen	L33
MJ006	c4_ma_dq<0>	ma_dq<0>	R37
MN006	c4_ma_dq<1>	ma_dq<1>	M42
MJ031	c4_ma_dq<10>	ma_dq<10>	V34
MN031	c4_ma_dq<11>	ma_dq<11>	U35
LN031	c4_ma_dq<12>	ma_dq<12>	AB30
LN036	c4_ma_dq<13>	ma_dq<13>	AA31
LU036	c4_ma_dq<14>	ma_dq<14>	Y34
LU031	c4_ma_dq<15>	ma_dq<15>	Y32
PN066	c4_ma_dq<16>	ma_dq<16>	D40
PJ066	c4_ma_dq<17>	ma_dq<17>	C39
PN071	c4_ma_dq<18>	ma_dq<18>	B38

Table 4-1. Signal I/Os (Page 7 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
PJ071	c4_ma_dq<19>	ma_dq<19>	D36
MJ011	c4_ma_dq<2>	ma_dq<2>	N37
RJ066	c4_ma_dq<20>	ma_dq<20>	A41
RJ071	c4_ma_dq<21>	ma_dq<21>	A39
RE066	c4_ma_dq<22>	ma_dq<22>	G35
RE071	c4_ma_dq<23>	ma_dq<23>	E35
PN106	c4_ma_dq<24>	ma_dq<24>	C31
PJ106	c4_ma_dq<25>	ma_dq<25>	A33
PN111	c4_ma_dq<26>	ma_dq<26>	A31
PJ111	c4_ma_dq<27>	ma_dq<27>	E31
RE106	c4_ma_dq<28>	ma_dq<28>	E29
RJ106	c4_ma_dq<29>	ma_dq<29>	C29
MN011	c4_ma_dq<3>	ma_dq<3>	P38
RE111	c4_ma_dq<30>	ma_dq<30>	G29
RJ111	c4_ma_dq<31>	ma_dq<31>	B30
NA106	c4_ma_dq<32>	ma_dq<32>	D28
MU111	c4_ma_dq<33>	ma_dq<33>	B28
MU106	c4_ma_dq<34>	ma_dq<34>	F26
NA111	c4_ma_dq<35>	ma_dq<35>	C25
NN111	c4_ma_dq<36>	ma_dq<36>	A27
NN106	c4_ma_dq<37>	ma_dq<37>	H28
NU111	c4_ma_dq<38>	ma_dq<38>	A25
NU106	c4_ma_dq<39>	ma_dq<39>	G25
LU006	c4_ma_dq<4>	ma_dq<4>	T36
PJ131	c4_ma_dq<40>	ma_dq<40>	F24
PJ136	c4_ma_dq<41>	ma_dq<41>	B22
PN131	c4_ma_dq<42>	ma_dq<42>	K22
PN136	c4_ma_dq<43>	ma_dq<43>	E21
RJ131	c4_ma_dq<44>	ma_dq<44>	D24
RE131	c4_ma_dq<45>	ma_dq<45>	A23
RE136	c4_ma_dq<46>	ma_dq<46>	F22
RJ136	c4_ma_dq<47>	ma_dq<47>	C21
NN131	c4_ma_dq<48>	ma_dq<48>	G21
NU136	c4_ma_dq<49>	ma_dq<49>	M20
LN011	c4_ma_dq<5>	ma_dq<5>	P42
NN136	c4_ma_dq<50>	ma_dq<50>	N21
NU131	c4_ma_dq<51>	ma_dq<51>	P22

Table 4-1. Signal I/Os (Page 8 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
NA131	c4_ma_dq<52>	ma_dq<52>	H22
MU131	c4_ma_dq<53>	ma_dq<53>	J25
NA136	c4_ma_dq<54>	ma_dq<54>	L25
MU136	c4_ma_dq<55>	ma_dq<55>	R21
NU091	c4_ma_dq<56>	ma_dq<56>	M24
NN096	c4_ma_dq<57>	ma_dq<57>	P24
NN091	c4_ma_dq<58>	ma_dq<58>	K26
NU096	c4_ma_dq<59>	ma_dq<59>	P26
LU011	c4_ma_dq<6>	ma_dq<6>	T38
NA096	c4_ma_dq<60>	ma_dq<60>	T22
MU096	c4_ma_dq<61>	ma_dq<61>	V22
NA091	c4_ma_dq<62>	ma_dq<62>	M26
MU091	c4_ma_dq<63>	ma_dq<63>	V26
RE091	c4_ma_dq<64>	ma_dq<64>	L31
RJ096	c4_ma_dq<65>	ma_dq<65>	C33
RJ091	c4_ma_dq<66>	ma_dq<66>	F32
RE096	c4_ma_dq<67>	ma_dq<67>	J33
PJ096	c4_ma_dq<68>	ma_dq<68>	D32
PN091	c4_ma_dq<69>	ma_dq<69>	F34
LN006	c4_ma_dq<7>	ma_dq<7>	R41
PN096	c4_ma_dq<70>	ma_dq<70>	A35
PJ091	c4_ma_dq<71>	ma_dq<71>	B36
MJ036	c4_ma_dq<8>	ma_dq<8>	W31
MN036	c4_ma_dq<9>	ma_dq<9>	W35
ME011	c4_ma_dqs_n<0>	ma_dqs_n<0>	N39
ME006	c4_ma_dqs_n<1>	ma_dqs_n<1>	P40
PU131	c4_ma_dqs_n<10>	ma_dqs_n<10>	H24
PU136	c4_ma_dqs_n<11>	ma_dqs_n<11>	C23
NJ131	c4_ma_dqs_n<12>	ma_dqs_n<12>	N23
NJ136	c4_ma_dqs_n<13>	ma_dqs_n<13>	K20
NJ091	c4_ma_dqs_n<14>	ma_dqs_n<14>	U25
NJ096	c4_ma_dqs_n<15>	ma_dqs_n<15>	U23
PU096	c4_ma_dqs_n<16>	ma_dqs_n<16>	B34
PU091	c4_ma_dqs_n<17>	ma_dqs_n<17>	G33
ME036	c4_ma_dqs_n<2>	ma_dqs_n<2>	U33
ME031	c4_ma_dqs_n<3>	ma_dqs_n<3>	AA33
PU071	c4_ma_dqs_n<4>	ma_dqs_n<4>	E37

Table 4-1. Signal I/Os (Page 9 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
PU066	c4_ma_dqs_n<5>	ma_dqs_n<5>	F38
PU106	c4_ma_dqs_n<6>	ma_dqs_n<6>	F30
PU111	c4_ma_dqs_n<7>	ma_dqs_n<7>	K30
NJ111	c4_ma_dqs_n<8>	ma_dqs_n<8>	D26
NJ106	c4_ma_dqs_n<9>	ma_dqs_n<9>	G27
MA011	c4_ma_dqs_p<0>	ma_dqs_p<0>	R39
MA006	c4_ma_dqs_p<1>	ma_dqs_p<1>	T40
RA131	c4_ma_dqs_p<10>	ma_dqs_p<10>	J23
RA136	c4_ma_dqs_p<11>	ma_dqs_p<11>	E23
NE131	c4_ma_dqs_p<12>	ma_dqs_p<12>	L23
NE136	c4_ma_dqs_p<13>	ma_dqs_p<13>	L21
NE091	c4_ma_dqs_p<14>	ma_dqs_p<14>	R25
NE096	c4_ma_dqs_p<15>	ma_dqs_p<15>	T24
RA096	c4_ma_dqs_p<16>	ma_dqs_p<16>	D34
RA091	c4_ma_dqs_p<17>	ma_dqs_p<17>	H32
MA036	c4_ma_dqs_p<2>	ma_dqs_p<2>	W33
MA031	c4_ma_dqs_p<3>	ma_dqs_p<3>	AB32
RA071	c4_ma_dqs_p<4>	ma_dqs_p<4>	C37
RA066	c4_ma_dqs_p<5>	ma_dqs_p<5>	E39
RA106	c4_ma_dqs_p<6>	ma_dqs_p<6>	H30
RA111	c4_ma_dqs_p<7>	ma_dqs_p<7>	J31
NE111	c4_ma_dqs_p<8>	ma_dqs_p<8>	B26
NE106	c4_ma_dqs_p<9>	ma_dqs_p<9>	E27
NE016	c4_ma0_clk_n<0>	ma0_clk_n<0>	L39
RA011	c4_ma0_clk_n<1>	ma0_clk_n<1>	J43
NJ016	c4_ma0_clk_p<0>	ma0_clk_p<0>	J39
RE011	c4_ma0_clk_p<1>	ma0_clk_p<1>	K42
NJ011	c4_ma0_cntl_cke<0>	ma0_cntl_cke<0>	K46
NJ006	c4_ma0_cntl_cke<1>	ma0_cntl_cke<1>	T32
NE041	c4_ma0_cntl_cke<2>	ma0_cntl_cke<2>	L45
PJ006	c4_ma0_cntl_cke<3>	ma0_cntl_cke<3>	P34
PA041	c4_ma0_cntl_csn<0>	ma0_cntl_csn<0>	A47
NE006	c4_ma0_cntl_csn<1>	ma0_cntl_csn<1>	U31
PN041	c4_ma0_cntl_csn<2>	ma0_cntl_csn<2>	A43
NU006	c4_ma0_cntl_csn<3>	ma0_cntl_csn<3>	T30
NU011	c4_ma0_cntl_odt<0>	ma0_cntl_odt<0>	H46
PJ016	c4_ma0_cntl_odt<1>	ma0_cntl_odt<1>	P32

Table 4-1. Signal I/Os (Page 10 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
NA001	c4_ma0_vrefdq	ma0_vrefdq	AA29
PN011	c4_ma1_clk_n<0>	ma1_clk_n<0>	H40
RA016	c4_ma1_clk_n<1>	ma1_clk_n<1>	J41
PJ011	c4_ma1_clk_p<0>	ma1_clk_p<0>	F40
RE016	c4_ma1_clk_p<1>	ma1_clk_p<1>	L41
PA011	c4_ma1_cntl_cke<0>	ma1_cntl_cke<0>	G45
PA006	c4_ma1_cntl_cke<1>	ma1_cntl_cke<1>	R33
NE036	c4_ma1_cntl_cke<2>	ma1_cntl_cke<2>	M44
NU041	c4_ma1_cntl_cke<3>	ma1_cntl_cke<3>	M34
PN016	c4_ma1_cntl_csn<0>	ma1_cntl_csn<0>	M36
RA006	c4_ma1_cntl_csn<1>	ma1_cntl_csn<1>	V30
NJ036	c4_ma1_cntl_csn<2>	ma1_cntl_csn<2>	N35
PN006	c4_ma1_cntl_csn<3>	ma1_cntl_csn<3>	W29
NE011	c4_ma1_cntl_odt<0>	ma1_cntl_odt<0>	K44
PA036	c4_ma1_cntl_odt<1>	ma1_cntl_odt<1>	N31
NA011	c4_ma1_vrefdq	ma1_vrefdq	AC29
NA066	c4_masp_dq<0>	masp_dq<0>	U27
MU071	c4_masp_dq<1>	masp_dq<1>	R27
MU066	c4_masp_dq<2>	masp_dq<2>	V28
NA071	c4_masp_dq<3>	masp_dq<3>	K28
NU066	c4_masp_dq<4>	masp_dq<4>	M28
NN066	c4_masp_dq<5>	masp_dq<5>	N27
NN071	c4_masp_dq<6>	masp_dq<6>	L29
NU071	c4_masp_dq<7>	masp_dq<7>	J27
NJ066	c4_masp_dqs_n<0>	masp_dqs_n<0>	R29
NJ071	c4_masp_dqs_n<1>	masp_dqs_n<1>	P30
NE066	c4_masp_dqs_p<0>	masp_dqs_p<0>	T28
NE071	c4_masp_dqs_p<1>	masp_dqs_p<1>	N29
NA226	c4_mb_atst<0>	mb_atst<0>	M10
PJ186	c4_mb_atst<1>	mb_atst<1>	F10
PN226	c4_mb_cmd_a<0>	mb_cmd_a<0>	J09
NJ211	c4_mb_cmd_a<1>	mb_cmd_a<1>	H08
PA206	c4_mb_cmd_a<10>	mb_cmd_a<10>	K12
PE201	c4_mb_cmd_a<11>	mb_cmd_a<11>	B04
RE226	c4_mb_cmd_a<12>	mb_cmd_a<12>	J07
PJ206	c4_mb_cmd_a<13>	mb_cmd_a<13>	F08
PN206	c4_mb_cmd_a<14>	mb_cmd_a<14>	C05

Table 4-1. Signal I/Os (Page 11 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
NE231	c4_mb_cmd_a<15>	mb_cmd_a<15>	M08
PN236	c4_mb_cmd_a<2>	mb_cmd_a<2>	K10
PJ226	c4_mb_cmd_a<3>	mb_cmd_a<3>	H04
NJ206	c4_mb_cmd_a<4>	mb_cmd_a<4>	F02
RA211	c4_mb_cmd_a<5>	mb_cmd_a<5>	C01
NJ201	c4_mb_cmd_a<6>	mb_cmd_a<6>	E05
NU201	c4_mb_cmd_a<7>	mb_cmd_a<7>	D04
NU211	c4_mb_cmd_a<8>	mb_cmd_a<8>	L13
RA201	c4_mb_cmd_a<9>	mb_cmd_a<9>	B02
RE206	c4_mb_cmd_actn	mb_cmd_actn	G03
NJ236	c4_mb_cmd_ba<0>	mb_cmd_ba<0>	L07
NE211	c4_mb_cmd_ba<1>	mb_cmd_ba<1>	L09
RE201	c4_mb_cmd_ba<2>	mb_cmd_ba<2>	J11
RA231	c4_mb_cmd_casn	mb_cmd_casn	N11
RJ186	c4_mb_cmd_errn	mb_cmd_errn	G11
RE186	c4_mb_cmd_eventn	mb_cmd_eventn	H12
RE211	c4_mb_cmd_par	mb_cmd_par	G05
RA206	c4_mb_cmd_rasn	mb_cmd_rasn	Y18
PN186	c4_mb_cmd_resetn	mb_cmd_resetn	G09
PJ236	c4_mb_cmd_wen	mb_cmd_wen	M12
RJ176	c4_mb_dq<0>	mb_dq<0>	P18
RE176	c4_mb_dq<1>	mb_dq<1>	M18
KJ206	c4_mb_dq<10>	mb_dq<10>	V20
KE206	c4_mb_dq<11>	mb_dq<11>	AB16
LA211	c4_mb_dq<12>	mb_dq<12>	AA15
LA206	c4_mb_dq<13>	mb_dq<13>	T20
LE211	c4_mb_dq<14>	mb_dq<14>	W15
LE206	c4_mb_dq<15>	mb_dq<15>	U19
RJ151	c4_mb_dq<16>	mb_dq<16>	E19
RJ146	c4_mb_dq<17>	mb_dq<17>	A19
RE146	c4_mb_dq<18>	mb_dq<18>	C17
RE151	c4_mb_dq<19>	mb_dq<19>	D16
RJ171	c4_mb_dq<2>	mb_dq<2>	J17
PN146	c4_mb_dq<20>	mb_dq<20>	B20
PN151	c4_mb_dq<21>	mb_dq<21>	F18
PJ146	c4_mb_dq<22>	mb_dq<22>	A17
PJ151	c4_mb_dq<23>	mb_dq<23>	F16

Table 4-1. Signal I/Os (Page 12 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
MU176	c4_mb_dq<24>	mb_dq<24>	B06
NA176	c4_mb_dq<25>	mb_dq<25>	A07
NA171	c4_mb_dq<26>	mb_dq<26>	C07
MU171	c4_mb_dq<27>	mb_dq<27>	A11
NU176	c4_mb_dq<28>	mb_dq<28>	E11
NN171	c4_mb_dq<29>	mb_dq<29>	D08
RE171	c4_mb_dq<3>	mb_dq<3>	N19
NN176	c4_mb_dq<30>	mb_dq<30>	G13
NU171	c4_mb_dq<31>	mb_dq<31>	E13
MJ231	c4_mb_dq<32>	mb_dq<32>	P10
MN231	c4_mb_dq<33>	mb_dq<33>	V06
MN236	c4_mb_dq<34>	mb_dq<34>	T06
MJ236	c4_mb_dq<35>	mb_dq<35>	N05
LN231	c4_mb_dq<36>	mb_dq<36>	V10
LN236	c4_mb_dq<37>	mb_dq<37>	U09
LU236	c4_mb_dq<38>	mb_dq<38>	R09
LU231	c4_mb_dq<39>	mb_dq<39>	P06
PN176	c4_mb_dq<4>	mb_dq<4>	R19
KE236	c4_mb_dq<40>	mb_dq<40>	W05
KJ236	c4_mb_dq<41>	mb_dq<41>	U03
KE231	c4_mb_dq<42>	mb_dq<42>	Y04
KJ231	c4_mb_dq<43>	mb_dq<43>	U01
LA231	c4_mb_dq<44>	mb_dq<44>	R05
LA236	c4_mb_dq<45>	mb_dq<45>	T04
LE236	c4_mb_dq<46>	mb_dq<46>	V04
LE231	c4_mb_dq<47>	mb_dq<47>	V02
HU236	c4_mb_dq<48>	mb_dq<48>	AC05
JA236	c4_mb_dq<49>	mb_dq<49>	AA05
PJ171	c4_mb_dq<5>	mb_dq<5>	D20
JA231	c4_mb_dq<50>	mb_dq<50>	AB06
HU231	c4_mb_dq<51>	mb_dq<51>	AD06
JN236	c4_mb_dq<52>	mb_dq<52>	Y02
JN231	c4_mb_dq<53>	mb_dq<53>	W01
JU236	c4_mb_dq<54>	mb_dq<54>	AD04
JU231	c4_mb_dq<55>	mb_dq<55>	AE03
JN211	c4_mb_dq<56>	mb_dq<56>	AA07
JU206	c4_mb_dq<57>	mb_dq<57>	Y08

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Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
JN206	c4_mb_dq<58>	mb_dq<58>	AB10
JU211	c4_mb_dq<59>	mb_dq<59>	W09
PJ176	c4_mb_dq<6>	mb_dq<6>	M16
JA206	c4_mb_dq<60>	mb_dq<60>	W07
HU211	c4_mb_dq<61>	mb_dq<61>	AE07
JA211	c4_mb_dq<62>	mb_dq<62>	AC11
HU206	c4_mb_dq<63>	mb_dq<63>	AE11
NN151	c4_mb_dq<64>	mb_dq<64>	B14
NU151	c4_mb_dq<65>	mb_dq<65>	C13
NN146	c4_mb_dq<66>	mb_dq<66>	A15
NU146	c4_mb_dq<67>	mb_dq<67>	C15
NA151	c4_mb_dq<68>	mb_dq<68>	B12
NA146	c4_mb_dq<69>	mb_dq<69>	D12
PN171	c4_mb_dq<7>	mb_dq<7>	G19
MU146	c4_mb_dq<70>	mb_dq<70>	J15
MU151	c4_mb_dq<71>	mb_dq<71>	L15
KJ211	c4_mb_dq<8>	mb_dq<8>	Y16
KE211	c4_mb_dq<9>	mb_dq<9>	AC17
PU171	c4_mb_dqs_n<0>	mb_dqs_n<0>	J19
PU176	c4_mb_dqs_n<1>	mb_dqs_n<1>	L17
KU236	c4_mb_dqs_n<10>	mb_dqs_n<10>	P02
KU231	c4_mb_dqs_n<11>	mb_dqs_n<11>	N03
JJ236	c4_mb_dqs_n<12>	mb_dqs_n<12>	AB02
JJ231	c4_mb_dqs_n<13>	mb_dqs_n<13>	AA03
JJ211	c4_mb_dqs_n<14>	mb_dqs_n<14>	AC09
JJ206	c4_mb_dqs_n<15>	mb_dqs_n<15>	AB08
NJ146	c4_mb_dqs_n<16>	mb_dqs_n<16>	H14
NJ151	c4_mb_dqs_n<17>	mb_dqs_n<17>	E15
KU211	c4_mb_dqs_n<2>	mb_dqs_n<2>	AA19
KU206	c4_mb_dqs_n<3>	mb_dqs_n<3>	AB18
PU151	c4_mb_dqs_n<4>	mb_dqs_n<4>	H16
PU146	c4_mb_dqs_n<5>	mb_dqs_n<5>	B18
NJ171	c4_mb_dqs_n<6>	mb_dqs_n<6>	C09
NJ176	c4_mb_dqs_n<7>	mb_dqs_n<7>	D10
ME231	c4_mb_dqs_n<8>	mb_dqs_n<8>	N07
ME236	c4_mb_dqs_n<9>	mb_dqs_n<9>	U07
RA171	c4_mb_dqs_p<0>	mb_dqs_p<0>	H20

Table 4-1. Signal I/Os (Page 14 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
RA176	c4_mb_dqs_p<1>	mb_dqs_p<1>	K18
KN236	c4_mb_dqs_p<10>	mb_dqs_p<10>	R01
KN231	c4_mb_dqs_p<11>	mb_dqs_p<11>	R03
JE236	c4_mb_dqs_p<12>	mb_dqs_p<12>	AC01
JE231	c4_mb_dqs_p<13>	mb_dqs_p<13>	AC03
JE211	c4_mb_dqs_p<14>	mb_dqs_p<14>	AE09
JE206	c4_mb_dqs_p<15>	mb_dqs_p<15>	AD08
NE146	c4_mb_dqs_p<16>	mb_dqs_p<16>	K14
NE151	c4_mb_dqs_p<17>	mb_dqs_p<17>	F14
KN211	c4_mb_dqs_p<2>	mb_dqs_p<2>	Y20
KN206	c4_mb_dqs_p<3>	mb_dqs_p<3>	AC19
RA151	c4_mb_dqs_p<4>	mb_dqs_p<4>	G17
RA146	c4_mb_dqs_p<5>	mb_dqs_p<5>	D18
NE171	c4_mb_dqs_p<6>	mb_dqs_p<6>	A09
NE176	c4_mb_dqs_p<7>	mb_dqs_p<7>	B10
MA231	c4_mb_dqs_p<8>	mb_dqs_p<8>	P08
MA236	c4_mb_dqs_p<9>	mb_dqs_p<9>	T08
PJ201	c4_mb0_clk_n<0>	mb0_clk_n<0>	F06
RE236	c4_mb0_clk_n<1>	mb0_clk_n<1>	N15
PN201	c4_mb0_clk_p<0>	mb0_clk_p<0>	E07
RA236	c4_mb0_clk_p<1>	mb0_clk_p<1>	P14
PE211	c4_mb0_cntl_cke<0>	mb0_cntl_cke<0>	E03
NE226	c4_mb0_cntl_cke<1>	mb0_cntl_cke<1>	L05
PA201	c4_mb0_cntl_cke<2>	mb0_cntl_cke<2>	A03
PA226	c4_mb0_cntl_cke<3>	mb0_cntl_cke<3>	N13
PN231	c4_mb0_cntl_csn<0>	mb0_cntl_csn<0>	K02
PA211	c4_mb0_cntl_csn<1>	mb0_cntl_csn<1>	R17
PE236	c4_mb0_cntl_csn<2>	mb0_cntl_csn<2>	L01
NU226	c4_mb0_cntl_csn<3>	mb0_cntl_csn<3>	U17
PE226	c4_mb0_cntl_odt<0>	mb0_cntl_odt<0>	J01
PJ231	c4_mb0_cntl_odt<1>	mb0_cntl_odt<1>	T16
HN201	c4_mb0_vrefdq	mb0_vrefdq	AB14
PA236	c4_mb1_clk_n<0>	mb1_clk_n<0>	H06
PA231	c4_mb1_clk_n<1>	mb1_clk_n<1>	U15
NU236	c4_mb1_clk_p<0>	mb1_clk_p<0>	K06
NU231	c4_mb1_clk_p<1>	mb1_clk_p<1>	T14
RA226	c4_mb1_cntl_cke<0>	mb1_cntl_cke<0>	J03

Table 4-1. Signal I/Os (Page 15 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
NU206	c4_mb1_cntl_cke<1>	mb1_cntl_cke<1>	P16
PJ211	c4_mb1_cntl_cke<2>	mb1_cntl_cke<2>	D02
NJ231	c4_mb1_cntl_cke<3>	mb1_cntl_cke<3>	R13
RE231	c4_mb1_cntl_csn<0>	mb1_cntl_csn<0>	K04
NE206	c4_mb1_cntl_csn<1>	mb1_cntl_csn<1>	W17
NJ226	c4_mb1_cntl_csn<2>	mb1_cntl_csn<2>	M02
NE201	c4_mb1_cntl_csn<3>	mb1_cntl_csn<3>	V18
PN211	c4_mb1_cntl_odt<0>	mb1_cntl_odt<0>	G01
NE236	c4_mb1_cntl_odt<1>	mb1_cntl_odt<1>	M04
HN206	c4_mb1_vrefdq	mb1_vrefdq	AD14
MN211	c4_mbsp_dq<0>	mbsp_dq<0>	V14
MJ211	c4_mbsp_dq<1>	mbsp_dq<1>	T12
MN206	c4_mbsp_dq<2>	mbsp_dq<2>	R11
MJ206	c4_mbsp_dq<3>	mbsp_dq<3>	AD12
LN206	c4_mbsp_dq<4>	mbsp_dq<4>	W13
LN211	c4_mbsp_dq<5>	mbsp_dq<5>	AA13
LU206	c4_mbsp_dq<6>	mbsp_dq<6>	AC13
LU211	c4_mbsp_dq<7>	mbsp_dq<7>	U11
ME206	c4_mbsp_dqs_n<0>	mbsp_dqs_n<0>	Y10
ME211	c4_mbsp_dqs_n<1>	mbsp_dqs_n<1>	V12
MA206	c4_mbsp_dqs_p<0>	mbsp_dqs_p<0>	AA11
MA211	c4_mbsp_dqs_p<1>	mbsp_dqs_p<1>	Y12
CJ226	c4_mc_atst<0>	mc_atst<0>	AP14
BA186	c4_mc_atst<1>	mc_atst<1>	BM04
AJ236	c4_mc_cmd_a<0>	mc_cmd_a<0>	AW09
BE236	c4_mc_cmd_a<1>	mc_cmd_a<1>	BA09
AE226	c4_mc_cmd_a<10>	mc_cmd_a<10>	BB04
BN211	c4_mc_cmd_a<11>	mc_cmd_a<11>	BA11
BJ226	c4_mc_cmd_a<12>	mc_cmd_a<12>	BA07
BA236	c4_mc_cmd_a<13>	mc_cmd_a<13>	AW13
BA206	c4_mc_cmd_a<14>	mc_cmd_a<14>	BB12
AE201	c4_mc_cmd_a<15>	mc_cmd_a<15>	BE05
AU211	c4_mc_cmd_a<2>	mc_cmd_a<2>	BC09
BN236	c4_mc_cmd_a<3>	mc_cmd_a<3>	AY08
AJ211	c4_mc_cmd_a<4>	mc_cmd_a<4>	BD08
CA211	c4_mc_cmd_a<5>	mc_cmd_a<5>	BB10
BE226	c4_mc_cmd_a<6>	mc_cmd_a<6>	AY12

Table 4-1. Signal I/Os (Page 16 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
BN226	c4_mc_cmd_a<7>	mc_cmd_a<7>	AW11
CE206	c4_mc_cmd_a<8>	mc_cmd_a<8>	AN17
AU206	c4_mc_cmd_a<9>	mc_cmd_a<9>	BD10
BA211	c4_mc_cmd_actn	mc_cmd_actn	BJ03
AJ206	c4_mc_cmd_ba<0>	mc_cmd_ba<0>	BG05
AE236	c4_mc_cmd_ba<1>	mc_cmd_ba<1>	AY06
BJ201	c4_mc_cmd_ba<2>	mc_cmd_ba<2>	BL05
AE206	c4_mc_cmd_casn	mc_cmd_casn	BE03
AA186	c4_mc_cmd_errn	mc_cmd_errn	BK02
AE186	c4_mc_cmd_eventn	mc_cmd_eventn	BK06
BE201	c4_mc_cmd_par	mc_cmd_par	BH06
BN231	c4_mc_cmd_rasn	mc_cmd_rasn	AV10
AU186	c4_mc_cmd_resetn	mc_cmd_resetn	BF06
BN206	c4_mc_cmd_wen	mc_cmd_wen	BG03
BU176	c4_mc_dq<0>	mc_dq<0>	AU19
BN176	c4_mc_dq<1>	mc_dq<1>	AW19
EE211	c4_mc_dq<10>	mc_dq<10>	AN19
EE206	c4_mc_dq<11>	mc_dq<11>	AL19
FA211	c4_mc_dq<12>	mc_dq<12>	AL13
FE206	c4_mc_dq<13>	mc_dq<13>	AK14
FA206	c4_mc_dq<14>	mc_dq<14>	AT18
FE211	c4_mc_dq<15>	mc_dq<15>	AJ15
AU151	c4_mc_dq<16>	mc_dq<16>	BF16
BA146	c4_mc_dq<17>	mc_dq<17>	BG17
BA151	c4_mc_dq<18>	mc_dq<18>	BB14
AU146	c4_mc_dq<19>	mc_dq<19>	BL17
BU171	c4_mc_dq<2>	mc_dq<2>	BC17
AE146	c4_mc_dq<20>	mc_dq<20>	BM16
AE151	c4_mc_dq<21>	mc_dq<21>	BK14
AA146	c4_mc_dq<22>	mc_dq<22>	BJ15
AA151	c4_mc_dq<23>	mc_dq<23>	BH14
AE171	c4_mc_dq<24>	mc_dq<24>	BM08
AA176	c4_mc_dq<25>	mc_dq<25>	BE11
AA171	c4_mc_dq<26>	mc_dq<26>	BL07
AE176	c4_mc_dq<27>	mc_dq<27>	BJ09
AU176	c4_mc_dq<28>	mc_dq<28>	BD12
AU171	c4_mc_dq<29>	mc_dq<29>	BL09

Table 4-1. Signal I/Os (Page 17 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
BN171	c4_mc_dq<3>	mc_dq<3>	BA17
BA176	c4_mc_dq<30>	mc_dq<30>	BF08
BA171	c4_mc_dq<31>	mc_dq<31>	BK10
CU206	c4_mc_dq<32>	mc_dq<32>	AV08
DA211	c4_mc_dq<33>	mc_dq<33>	AU07
DA206	c4_mc_dq<34>	mc_dq<34>	AW03
CU211	c4_mc_dq<35>	mc_dq<35>	AV02
DN206	c4_mc_dq<36>	mc_dq<36>	AT10
DN211	c4_mc_dq<37>	mc_dq<37>	AT08
DU206	c4_mc_dq<38>	mc_dq<38>	AR07
DU211	c4_mc_dq<39>	mc_dq<39>	AP06
CJ176	c4_mc_dq<4>	mc_dq<4>	AW17
CU231	c4_mc_dq<40>	mc_dq<40>	AW01
CU236	c4_mc_dq<41>	mc_dq<41>	AT02
DA236	c4_mc_dq<42>	mc_dq<42>	AN01
DA231	c4_mc_dq<43>	mc_dq<43>	AR01
DU231	c4_mc_dq<44>	mc_dq<44>	AU03
DU236	c4_mc_dq<45>	mc_dq<45>	AT04
DN231	c4_mc_dq<46>	mc_dq<46>	AL03
DN236	c4_mc_dq<47>	mc_dq<47>	AM04
FE236	c4_mc_dq<48>	mc_dq<48>	AN07
FA236	c4_mc_dq<49>	mc_dq<49>	AK06
CN176	c4_mc_dq<5>	mc_dq<5>	AV18
FE231	c4_mc_dq<50>	mc_dq<50>	AG01
FA231	c4_mc_dq<51>	mc_dq<51>	AE01
EJ231	c4_mc_dq<52>	mc_dq<52>	AM06
EE236	c4_mc_dq<53>	mc_dq<53>	AL05
EJ236	c4_mc_dq<54>	mc_dq<54>	AH04
EE231	c4_mc_dq<55>	mc_dq<55>	AJ05
FU231	c4_mc_dq<56>	mc_dq<56>	AF04
FN231	c4_mc_dq<57>	mc_dq<57>	AH08
FN236	c4_mc_dq<58>	mc_dq<58>	AL09
FU236	c4_mc_dq<59>	mc_dq<59>	AG09
CJ171	c4_mc_dq<6>	mc_dq<6>	BD16
GN231	c4_mc_dq<60>	mc_dq<60>	AF02
GN236	c4_mc_dq<61>	mc_dq<61>	AG05
GJ236	c4_mc_dq<62>	mc_dq<62>	AF06

Table 4-1. Signal I/Os (Page 18 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
GJ231	c4_mc_dq<63>	mc_dq<63>	AF10
CN151	c4_mc_dq<64>	mc_dq<64>	BM10
CJ146	c4_mc_dq<65>	mc_dq<65>	BJ11
CJ151	c4_mc_dq<66>	mc_dq<66>	BF14
CN146	c4_mc_dq<67>	mc_dq<67>	BH12
BN151	c4_mc_dq<68>	mc_dq<68>	BG11
BN146	c4_mc_dq<69>	mc_dq<69>	BL13
CN171	c4_mc_dq<7>	mc_dq<7>	AY14
BU151	c4_mc_dq<70>	mc_dq<70>	BG13
BU146	c4_mc_dq<71>	mc_dq<71>	BL15
EJ206	c4_mc_dq<8>	mc_dq<8>	AP18
EJ211	c4_mc_dq<9>	mc_dq<9>	AM14
CA171	c4_mc_dqs_n<0>	mc_dqs_n<0>	BA19
CA176	c4_mc_dqs_n<1>	mc_dqs_n<1>	BA15
DE231	c4_mc_dqs_n<10>	mc_dqs_n<10>	AP02
DE236	c4_mc_dqs_n<11>	mc_dqs_n<11>	AP04
EN236	c4_mc_dqs_n<12>	mc_dqs_n<12>	AJ03
EN231	c4_mc_dqs_n<13>	mc_dqs_n<13>	AK02
GA231	c4_mc_dqs_n<14>	mc_dqs_n<14>	AK08
GA236	c4_mc_dqs_n<15>	mc_dqs_n<15>	AJ07
CA146	c4_mc_dqs_n<16>	mc_dqs_n<16>	BM12
CA151	c4_mc_dqs_n<17>	mc_dqs_n<17>	BE13
EN206	c4_mc_dqs_n<2>	mc_dqs_n<2>	AK18
EN211	c4_mc_dqs_n<3>	mc_dqs_n<3>	AM16
AN151	c4_mc_dqs_n<4>	mc_dqs_n<4>	BE15
AN146	c4_mc_dqs_n<5>	mc_dqs_n<5>	BJ17
AN171	c4_mc_dqs_n<6>	mc_dqs_n<6>	BH08
AN176	c4_mc_dqs_n<7>	mc_dqs_n<7>	BF10
DE206	c4_mc_dqs_n<8>	mc_dqs_n<8>	AY04
DE211	c4_mc_dqs_n<9>	mc_dqs_n<9>	AV06
CE171	c4_mc_dqs_p<0>	mc_dqs_p<0>	BB18
CE176	c4_mc_dqs_p<1>	mc_dqs_p<1>	AY16
DJ231	c4_mc_dqs_p<10>	mc_dqs_p<10>	AN03
DJ236	c4_mc_dqs_p<11>	mc_dqs_p<11>	AR05
EU236	c4_mc_dqs_p<12>	mc_dqs_p<12>	AH02
EU231	c4_mc_dqs_p<13>	mc_dqs_p<13>	AL01
GE231	c4_mc_dqs_p<14>	mc_dqs_p<14>	AM08

Table 4-1. Signal I/Os (Page 19 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
GE236	c4_mc_dqs_p<15>	mc_dqs_p<15>	AG07
CE146	c4_mc_dqs_p<16>	mc_dqs_p<16>	BK12
CE151	c4_mc_dqs_p<17>	mc_dqs_p<17>	BC13
EU206	c4_mc_dqs_p<2>	mc_dqs_p<2>	AL17
EU211	c4_mc_dqs_p<3>	mc_dqs_p<3>	AK16
AJ151	c4_mc_dqs_p<4>	mc_dqs_p<4>	BC15
AJ146	c4_mc_dqs_p<5>	mc_dqs_p<5>	BH16
AJ171	c4_mc_dqs_p<6>	mc_dqs_p<6>	BJ07
AJ176	c4_mc_dqs_p<7>	mc_dqs_p<7>	BG09
DJ206	c4_mc_dqs_p<8>	mc_dqs_p<8>	AW05
DJ211	c4_mc_dqs_p<9>	mc_dqs_p<9>	AU05
AJ231	c4_mc0_clk_n<0>	mc0_clk_n<0>	BC05
CE236	c4_mc0_clk_n<1>	mc0_clk_n<1>	AT12
AE231	c4_mc0_clk_p<0>	mc0_clk_p<0>	BB06
CA236	c4_mc0_clk_p<1>	mc0_clk_p<1>	AR13
AU236	c4_mc0_cntl_cke<0>	mc0_cntl_cke<0>	AV14
BA226	c4_mc0_cntl_cke<1>	mc0_cntl_cke<1>	BG01
CE226	c4_mc0_cntl_cke<2>	mc0_cntl_cke<2>	AU11
CA201	c4_mc0_cntl_cke<3>	mc0_cntl_cke<3>	BM02
BJ236	c4_mc0_cntl_csn<0>	mc0_cntl_csn<0>	AT16
BJ211	c4_mc0_cntl_csn<1>	mc0_cntl_csn<1>	BF02
CE201	c4_mc0_cntl_csn<2>	mc0_cntl_csn<2>	AR17
AE211	c4_mc0_cntl_csn<3>	mc0_cntl_csn<3>	BD02
CA206	c4_mc0_cntl_odt<0>	mc0_cntl_odt<0>	BD04
BJ206	c4_mc0_cntl_odt<1>	mc0_cntl_odt<1>	BL01
GU201	c4_mc0_vrefdq	mc0_vrefdq	AF12
AU201	c4_mc1_clk_n<0>	mc1_clk_n<0>	BE07
CE231	c4_mc1_clk_n<1>	mc1_clk_n<1>	AN15
BA201	c4_mc1_clk_p<0>	mc1_clk_p<0>	BC07
CA231	c4_mc1_clk_p<1>	mc1_clk_p<1>	AR15
AU226	c4_mc1_cntl_cke<0>	mc1_cntl_cke<0>	AV16
BN201	c4_mc1_cntl_cke<1>	mc1_cntl_cke<1>	BH04
CA226	c4_mc1_cntl_cke<2>	mc1_cntl_cke<2>	AU13
AJ201	c4_mc1_cntl_cke<3>	mc1_cntl_cke<3>	BK04
CE211	c4_mc1_cntl_csn<0>	mc1_cntl_csn<0>	BA03
AU231	c4_mc1_cntl_csn<1>	mc1_cntl_csn<1>	BC01
AJ226	c4_mc1_cntl_csn<2>	mc1_cntl_csn<2>	BB02

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Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
BJ231	c4_mc1_cntl_csn<3>	mc1_cntl_csn<3>	BA01
BA231	c4_mc1_cntl_odt<0>	mc1_cntl_odt<0>	AU15
BE211	c4_mc1_cntl_odt<1>	mc1_cntl_odt<1>	BJ01
GU206	c4_mc1_vrefdq	mc1_vrefdq	AG13
GN206	c4_mcsp_dq<0>	mcsp_dq<0>	AH12
GJ211	c4_mcsp_dq<1>	mcsp_dq<1>	AJ11
GN211	c4_mcsp_dq<2>	mcsp_dq<2>	AH10
GJ206	c4_mcsp_dq<3>	mcsp_dq<3>	AP10
FU211	c4_mcsp_dq<4>	mcsp_dq<4>	AJ13
FN206	c4_mcsp_dq<5>	mcsp_dq<5>	AP12
FN211	c4_mcsp_dq<6>	mcsp_dq<6>	AM12
FU206	c4_mcsp_dq<7>	mcsp_dq<7>	AN11
GA211	c4_mcsp_dqs_n<0>	mcsp_dqs_n<0>	AK10
GA206	c4_mcsp_dqs_n<1>	mcsp_dqs_n<1>	AR09
GE211	c4_mcsp_dqs_p<0>	mcsp_dqs_p<0>	AL11
GE206	c4_mcsp_dqs_p<1>	mcsp_dqs_p<1>	AN09
BA056	c4_md_atst<0>	md_atst<0>	BM40
CJ016	c4_md_atst<1>	md_atst<1>	BD40
BA031	c4_md_cmd_a<0>	md_cmd_a<0>	BL41
BJ011	c4_md_cmd_a<1>	md_cmd_a<1>	BG41
BE016	c4_md_cmd_a<10>	md_cmd_a<10>	BK44
BN031	c4_md_cmd_a<11>	md_cmd_a<11>	BE37
BJ016	c4_md_cmd_a<12>	md_cmd_a<12>	BK42
BN041	c4_md_cmd_a<13>	md_cmd_a<13>	BB34
AJ041	c4_md_cmd_a<14>	md_cmd_a<14>	BH36
AE036	c4_md_cmd_a<15>	md_cmd_a<15>	BE43
AE006	c4_md_cmd_a<2>	md_cmd_a<2>	BB40
AE041	c4_md_cmd_a<3>	md_cmd_a<3>	BF42
BA006	c4_md_cmd_a<4>	md_cmd_a<4>	BJ41
BN011	c4_md_cmd_a<5>	md_cmd_a<5>	BE39
BA036	c4_md_cmd_a<6>	md_cmd_a<6>	BG37
AJ036	c4_md_cmd_a<7>	md_cmd_a<7>	BK38
BJ041	c4_md_cmd_a<8>	md_cmd_a<8>	BC33
AU011	c4_md_cmd_a<9>	md_cmd_a<9>	BF38
BA011	c4_md_cmd_actn	md_cmd_actn	BB36
BN016	c4_md_cmd_ba<0>	md_cmd_ba<0>	BJ43
AJ031	c4_md_cmd_ba<1>	md_cmd_ba<1>	BM42

Table 4-1. Signal I/Os (Page 21 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
BN006	c4_md_cmd_ba<2>	md_cmd_ba<2>	BG43
AU031	c4_md_cmd_casn	md_cmd_casn	BB44
AA056	c4_md_cmd_errn	md_cmd_errn	BM44
AE056	c4_md_cmd_eventn	md_cmd_eventn	BL37
BN036	c4_md_cmd_par	md_cmd_par	BH38
CA031	c4_md_cmd_rasn	md_cmd_rasn	BL45
AU056	c4_md_cmd_resetn	md_cmd_resetn	BD34
CE041	c4_md_cmd_wen	md_cmd_wen	BH44
DA006	c4_md_dq<0>	md_dq<0>	AW35
DA011	c4_md_dq<1>	md_dq<1>	AV34
CU036	c4_md_dq<10>	md_dq<10>	AT34
CU031	c4_md_dq<11>	md_dq<11>	AU35
DU031	c4_md_dq<12>	md_dq<12>	AM30
DU036	c4_md_dq<13>	md_dq<13>	AP30
DN031	c4_md_dq<14>	md_dq<14>	AR35
DN036	c4_md_dq<15>	md_dq<15>	AW33
AE071	c4_md_dq<16>	md_dq<16>	BC31
AA071	c4_md_dq<17>	md_dq<17>	BF32
AE066	c4_md_dq<18>	md_dq<18>	BB30
AA066	c4_md_dq<19>	md_dq<19>	BE31
CU006	c4_md_dq<2>	md_dq<2>	BB38
AU071	c4_md_dq<20>	md_dq<20>	BG33
AU066	c4_md_dq<21>	md_dq<21>	BD32
BA066	c4_md_dq<22>	md_dq<22>	BF34
BA071	c4_md_dq<23>	md_dq<23>	BK34
AE091	c4_md_dq<24>	md_dq<24>	BE27
AA096	c4_md_dq<25>	md_dq<25>	BM26
AA091	c4_md_dq<26>	md_dq<26>	BM28
AE096	c4_md_dq<27>	md_dq<27>	BG29
AU096	c4_md_dq<28>	md_dq<28>	BL25
BA096	c4_md_dq<29>	md_dq<29>	BK26
CU011	c4_md_dq<3>	md_dq<3>	BA37
BA091	c4_md_dq<30>	md_dq<30>	BE29
AU091	c4_md_dq<31>	md_dq<31>	BL29
AA106	c4_md_dq<32>	md_dq<32>	BJ25
AE111	c4_md_dq<33>	md_dq<33>	BD26
AE106	c4_md_dq<34>	md_dq<34>	BC25

Table 4-1. Signal I/Os (Page 22 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
AA111	c4_md_dq<35>	md_dq<35>	BK22
BA111	c4_md_dq<36>	md_dq<36>	BF26
AU106	c4_md_dq<37>	md_dq<37>	BG25
BA106	c4_md_dq<38>	md_dq<38>	BM24
AU111	c4_md_dq<39>	md_dq<39>	BL21
DU006	c4_md_dq<4>	md_dq<4>	AY38
BA131	c4_md_dq<40>	md_dq<40>	BA25
AU131	c4_md_dq<41>	md_dq<41>	BF22
BA136	c4_md_dq<42>	md_dq<42>	BM18
AU136	c4_md_dq<43>	md_dq<43>	BK18
AE131	c4_md_dq<44>	md_dq<44>	BD24
AA131	c4_md_dq<45>	md_dq<45>	BH22
AE136	c4_md_dq<46>	md_dq<46>	BE21
AA136	c4_md_dq<47>	md_dq<47>	BG21
BU131	c4_md_dq<48>	md_dq<48>	BE23
BN136	c4_md_dq<49>	md_dq<49>	BC21
DU011	c4_md_dq<5>	md_dq<5>	AY40
BN131	c4_md_dq<50>	md_dq<50>	BB22
BU136	c4_md_dq<51>	md_dq<51>	BA23
CN131	c4_md_dq<52>	md_dq<52>	BG19
CJ136	c4_md_dq<53>	md_dq<53>	BF18
CJ131	c4_md_dq<54>	md_dq<54>	BC23
CN136	c4_md_dq<55>	md_dq<55>	AY20
BN111	c4_md_dq<56>	md_dq<56>	AY22
BU111	c4_md_dq<57>	md_dq<57>	AT20
BN106	c4_md_dq<58>	md_dq<58>	AR25
BU106	c4_md_dq<59>	md_dq<59>	AP26
DN011	c4_md_dq<6>	md_dq<6>	AY36
CN111	c4_md_dq<60>	md_dq<60>	AW21
CJ111	c4_md_dq<61>	md_dq<61>	AU21
CN106	c4_md_dq<62>	md_dq<62>	AR23
CJ106	c4_md_dq<63>	md_dq<63>	AT24
CN096	c4_md_dq<64>	md_dq<64>	BC29
CJ091	c4_md_dq<65>	md_dq<65>	BF30
CJ096	c4_md_dq<66>	md_dq<66>	BJ33
CN091	c4_md_dq<67>	md_dq<67>	AW29
BN096	c4_md_dq<68>	md_dq<68>	BL33

Table 4-1. Signal I/Os (Page 23 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
BU091	c4_md_dq<69>	md_dq<69>	BH30
DN006	c4_md_dq<7>	md_dq<7>	BC37
BN091	c4_md_dq<70>	md_dq<70>	BK30
BU096	c4_md_dq<71>	md_dq<71>	BM34
DA031	c4_md_dq<8>	md_dq<8>	AR31
DA036	c4_md_dq<9>	md_dq<9>	AU31
DE011	c4_md_dqs_n<0>	md_dqs_n<0>	BC39
DE006	c4_md_dqs_n<1>	md_dqs_n<1>	BC41
AN136	c4_md_dqs_n<10>	md_dqs_n<10>	BJ19
AN131	c4_md_dqs_n<11>	md_dqs_n<11>	BK20
CA131	c4_md_dqs_n<12>	md_dqs_n<12>	BD20
CA136	c4_md_dqs_n<13>	md_dqs_n<13>	BD18
CA106	c4_md_dqs_n<14>	md_dqs_n<14>	AU23
CA111	c4_md_dqs_n<15>	md_dqs_n<15>	AT22
CA096	c4_md_dqs_n<16>	md_dqs_n<16>	BL31
CA091	c4_md_dqs_n<17>	md_dqs_n<17>	BJ31
DE031	c4_md_dqs_n<2>	md_dqs_n<2>	AR33
DE036	c4_md_dqs_n<3>	md_dqs_n<3>	AT32
AN071	c4_md_dqs_n<4>	md_dqs_n<4>	BM36
AN066	c4_md_dqs_n<5>	md_dqs_n<5>	BG35
AN096	c4_md_dqs_n<6>	md_dqs_n<6>	BJ27
AN091	c4_md_dqs_n<7>	md_dqs_n<7>	BH28
AN111	c4_md_dqs_n<8>	md_dqs_n<8>	BL23
AN106	c4_md_dqs_n<9>	md_dqs_n<9>	BF24
DJ011	c4_md_dqs_p<0>	md_dqs_p<0>	BA39
DJ006	c4_md_dqs_p<1>	md_dqs_p<1>	BA41
AJ136	c4_md_dqs_p<10>	md_dqs_p<10>	BH20
AJ131	c4_md_dqs_p<11>	md_dqs_p<11>	BM20
CE131	c4_md_dqs_p<12>	md_dqs_p<12>	BB20
CE136	c4_md_dqs_p<13>	md_dqs_p<13>	BE19
CE106	c4_md_dqs_p<14>	md_dqs_p<14>	AV22
CE111	c4_md_dqs_p<15>	md_dqs_p<15>	AR21
CE096	c4_md_dqs_p<16>	md_dqs_p<16>	BM32
CE091	c4_md_dqs_p<17>	md_dqs_p<17>	BH32
DJ031	c4_md_dqs_p<2>	md_dqs_p<2>	AN33
DJ036	c4_md_dqs_p<3>	md_dqs_p<3>	AP32
AJ071	c4_md_dqs_p<4>	md_dqs_p<4>	BK36

Table 4-1. Signal I/Os (Page 24 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
AJ066	c4_md_dqs_p<5>	md_dqs_p<5>	BJ35
AJ096	c4_md_dqs_p<6>	md_dqs_p<6>	BG27
AJ091	c4_md_dqs_p<7>	md_dqs_p<7>	BK28
AJ111	c4_md_dqs_p<8>	md_dqs_p<8>	BJ23
AJ106	c4_md_dqs_p<9>	md_dqs_p<9>	BH24
BA041	c4_md0_clk_n<0>	md0_clk_n<0>	BJ39
AJ016	c4_md0_clk_n<1>	md0_clk_n<1>	BD42
AU041	c4_md0_clk_p<0>	md0_clk_p<0>	BL39
AE016	c4_md0_clk_p<1>	md0_clk_p<1>	BB42
CA011	c4_md0_cntl_cke<0>	md0_cntl_cke<0>	BG45
CA041	c4_md0_cntl_cke<1>	md0_cntl_cke<1>	AY30
AE031	c4_md0_cntl_cke<2>	md0_cntl_cke<2>	BD44
CA036	c4_md0_cntl_cke<3>	md0_cntl_cke<3>	BA33
BE006	c4_md0_cntl_csn<0>	md0_cntl_csn<0>	BJ47
CE031	c4_md0_cntl_csn<1>	md0_cntl_csn<1>	AV30
CE011	c4_md0_cntl_csn<2>	md0_cntl_csn<2>	BG47
AJ006	c4_md0_cntl_csn<3>	md0_cntl_csn<3>	AU29
BE031	c4_md0_cntl_odt<0>	md0_cntl_odt<0>	BM46
BJ036	c4_md0_cntl_odt<1>	md0_cntl_odt<1>	AY32
CJ001	c4_md0_vrefdq	md0_vrefdq	AN29
CE016	c4_md1_clk_n<0>	md1_clk_n<0>	BF40
AJ011	c4_md1_clk_n<1>	md1_clk_n<1>	AY44
CA016	c4_md1_clk_p<0>	md1_clk_p<0>	BH40
AE011	c4_md1_clk_p<1>	md1_clk_p<1>	BA43
AU016	c4_md1_cntl_cke<0>	md1_cntl_cke<0>	BK46
BJ006	c4_md1_cntl_cke<1>	md1_cntl_cke<1>	AV32
CA006	c4_md1_cntl_cke<2>	md1_cntl_cke<2>	BE45
BA016	c4_md1_cntl_cke<3>	md1_cntl_cke<3>	BA35
BJ031	c4_md1_cntl_csn<0>	md1_cntl_csn<0>	BD36
CE006	c4_md1_cntl_csn<1>	md1_cntl_csn<1>	AR29
BE041	c4_md1_cntl_csn<2>	md1_cntl_csn<2>	BE35
AU006	c4_md1_cntl_csn<3>	md1_cntl_csn<3>	AT28
CE036	c4_md1_cntl_odt<0>	md1_cntl_odt<0>	BH46
AU036	c4_md1_cntl_odt<1>	md1_cntl_odt<1>	BA31
CJ011	c4_md1_vrefdq	md1_vrefdq	AL29
CJ071	c4_mdsp_dq<0>	mdsp_dq<0>	AY28
CJ066	c4_mdsp_dq<1>	mdsp_dq<1>	BD28

Table 4-1. Signal I/Os (Page 25 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
CN066	c4_mdsp_dq<2>	mdsp_dq<2>	AT26
CN071	c4_mdsp_dq<3>	mdsp_dq<3>	AU27
BU071	c4_mdsp_dq<4>	mdsp_dq<4>	AV24
BU066	c4_mdsp_dq<5>	mdsp_dq<5>	BB28
BN066	c4_mdsp_dq<6>	mdsp_dq<6>	AW25
BN071	c4_mdsp_dq<7>	mdsp_dq<7>	AY24
CA071	c4_mdsp_dqs_n<0>	mdsp_dqs_n<0>	BB26
CA066	c4_mdsp_dqs_n<1>	mdsp_dqs_n<1>	AV26
CE071	c4_mdsp_dqs_p<0>	mdsp_dqs_p<0>	BA27
CE066	c4_mdsp_dqs_p<1>	mdsp_dqs_p<1>	AW27
HN226	c4_pll_bypass	pll_bypass	AE17
HE226	c4_rfu0	rfu0	AG15
HJ226	c4_rfu1	rfu1	AD16
LG016	c4_rfu_vsb0	scl_spr	AE47
KU016	c4_rfu_vsb1	sda_spr	AC47
KM011	c4_scl_mstr	scl_mstr	L47
KB011	c4_sda_mstr	sda_mstr	M46
GU211	c4_single_probe<0>	single_probe<0>	AJ19
HA236	c4_single_probe<1>	single_probe<1>	AH16
HE236	c4_single_probe<2>	single_probe<2>	AE15
HJ211	c4_therm_a	therm_a	AF14
HN211	c4_therm_b	therm_b	AE19
MU011	refavdd0	MA_REFAVDD	Y26
PA091	refavdd1	MA_REFAVDD	Y26
BJ091	refavdd10	MD_REFAVDD	AM26
BJ131	refavdd11	MD_REFAVDD	AM26
PA131	refavdd2	MA_REFAVDD	Y26
MU231	refavdd3	MB_REFAVDD	AD20
PA151	refavdd4	MB_REFAVDD	AD20
KA231	refavdd5	MB_REFAVDD	AD20
CN231	refavdd6	MC_REFAVDD	AM20
BJ151	refavdd7	MC_REFAVDD	AM20
FJ231	refavdd8	MC_REFAVDD	AM20
CN011	refavdd9	MD_REFAVDD	AM26
EG051	vmon_gnd	vmon_gnd	AL25
LU141	vmon_vcs	vmon_vcs	AA21
EB021	vmon_vdd	vmon_vdd	AL27

Table 4-1. Signal I/Os (Page 26 of 26)

Chip C4	Chip Signal Name	BGA Signal Name	BGA C4
DA146	vmon_vddr	vmon_vddr	AL21
KB046	vmon_vio	vmon_vio	AE27
JG076	vmon_vpp0	vmon_vpp0	AD24
GB076	vmon_vpp1	vmon_vpp1	AH24
LB051	vmon_vsb	vmon_vsb	AA25
MA096	vmon_vwl0	vmon_vwl0	AA23
DJ096	vmon_vwl1	vmon_vwl1	AN23

4.2 Power Rails

Table 4-2. Power Rails (Page 1 of 4)

Rail	BGA List
VIO	FG006 FG016 FG021 FG026 FG036 FG046 GG006 GG016 GG021 GG026 GG036 GG041 GG046 GG066 HG006 HG016 HG021 HG026 HG036 HG041 HG046 JU006 JU016 JU021 JU026 JU036 JU041 JU046
VSB	KB001 KB006 KB016 KB021 KB026 KB031 KB051 KM021 KM026 KM031 KM046 KM051 LB001 LB006 LB021 LB026 LB031 LB046
VCS	DN071 DN076 DN091 DN096 DN111 DN121 DN131 DN141 DN156 DN161 DN176 DN181 EB071 EB076 EB091 EB096 EB111 EB121 EB131 EB141 EB156 EB161 EB176 EB181 EU071 EU076 EU091 EU096 EU111 EU121 EU131 EU141 EU156 EU161 EU176 EU181 FG071 FG076 FG091 FG096 FG111 FG121 FG131 FG141 FG156 FG161 FG176 FG181 FU071 FU076 FU091 FU096 FU111 FU121 FU131 FU141 FU156 FU161 FU176 FU181 GG071 GG076 GG091 GG096 GG111 GG121 GG131 GG141 GG156 GG161 GG176 GG181 GU071 GU076 GU091 GU096 GU111 GU121 GU131 GU141 GU156 GU161 GU176 GU181 HG071 HG076 HG091 HG096 HG111 HG121 HG131 HG141 HG156 HG161 HG176 HG181 HU071 HU076 HU091 HU096 HU111 HU121 HU131 HU141 HU156 HU161 HU176 HU181 JG071 JG091 JG096 JG111 JG121 JG131 JG141 JG156 JG161 JG176 JG181 JU071 JU076 JU091 JU096 JU111 JU121 JU131 JU141 JU156 JU161 JU176 JU181 KB071 KB076 KB091 KB096 KB111 KB121 KB131 KB141 KB156 KB161 KB176 KB181 KM071 KM076 KM091 KM096 KM111 KM121 KM131 KM141 KM156 KM161 KM176 KM181 LB071 LB076 LB091 LB096 LB111 LB121 LB131 LB141 LB156 LB161 LB176 LB181 LG071 LG076 LG091 LG096 LG111 LG121 LG131 LG141 LG156 LG161 LG176 LG181 LU071 LU076 LU091 LU096 LU111 LU121 LU131 LU156 LU161 LU176 LU181

Table 4-2. Power Rails (Page 2 of 4)

Rail	BGA List
VDD	AE026 AE051 AE191 AE216 AJ026 AJ051 AJ056 AJ186 AJ191 AJ216 BA026 BA051 BA081 BA121 BA161 BA191 BA216 BJ026 BJ051 BJ056 BJ066 BJ076 BJ081 BJ086 BJ096 BJ106 BJ116 BJ121 BJ126 BJ136 BJ146 BJ156 BJ161 BJ166 BJ176 BJ186 BJ191 BJ216 BN026 BN051 BN056 BN081 BN121 BN161 BN186 BN191 BN216 CE051 CE056 CE186 CE191 CJ021 CJ026 CJ051 CJ056 CJ186 CJ191 CJ216 CJ221 CU021 CU051 CU056 CU076 CU081 CU086 CU101 CU116 CU121 CU126 CU141 CU156 CU161 CU166 CU186 CU191 CU221 DE021 DE046 DE051 DE056 DE061 DE066 DE071 DE076 DE081 DE086 DE091 DE096 DE101 DE106 DE111 DE116 DE121 DE126 DE131 DE136 DE141 DE146 DE151 DE156 DE161 DE166 DE171 DE176 DE181 DE186 DE191 DE196 DE221 DN046 DN051 DN056 DN061 DN066 DN081 DN086 DN101 DN106 DN116 DN126 DN136 DN146 DN151 DN166 DN171 DN186 DN191 DN196 EA201 EA216 EA221 EA226 EA231 EB011 EB016 EB026 EB031 EB036 EB041 EB046 EB051 EB056 EB061 EB066 EB081 EB086 EB101 EB106 EB116 EB126 EB136 EB146 EB151 EB166 EB171 EB186 EB191 EB196 EE221 EN221 EU051 EU056 EU061 EU066 EU081 EU086 EU101 EU106 EU116 EU126 EU136 EU146 EU151 EU166 EU171 EU186 EU191 EU196 FG011 FG031 FG051 FG056 FG061 FG066 FG081 FG086 FG101 FG106 FG116 FG126 FG136 FG146 FG151 FG166 FG171 FG186 FG191 FG196 FJ201 FJ216 FJ221 FJ226 FN221 FU051 FU056 FU061 FU066 FU081 FU086 FU101 FU106 FU116 FU126 FU136 FU146 FU151 FU166 FU171 FU186 FU191 FU196 GA221 GG011 GG031 GG081 GG086 GG101 GG106 GG116 GG126 GG136 GG146 GG151 GG166 GG171 GG186 GG191 GG196 GU051 GU056 GU061 GU066 GU081 GU086 GU101 GU106 GU116 GU126 GU136 GU146 GU151 GU166 GU171 GU186 GU191 GU196 HA201 HA206 HA211 HA221 HA231 HA241 HG011 HG031 HG051 HG056 HG061 HG066 HG081 HG086 HG101 HG106 HG116 HG126 HG136 HG146 HG151 HG166 HG171 HG186 HG191 HG196 HJ201 HJ206 HJ221 HJ231 HJ236 HJ241 HU051 HU056 HU061 HU066 HU081 HU086 HU101 HU106 HU116 HU126 HU136 HU146 HU151 HU166 HU171 HU186 HU191 HU196 JG051 JG056 JG061 JG066 JG081 JG086 JG101 JG106 JG116 JG126 JG136 JG146 JG151 JG166 JG171 JG186 JG191 JG196 JJ221 JU011 JU031 JU051 JU056 JU061 JU066 JU081 JU086 JU101 JU106 JU116 JU126 JU136 JU146 JU151 JU166 JU171 JU186 JU191 JU196 JU221 KA201 KA216 KA221 KA226 KB036 KB041 KB056 KB061 KB066 KB081 KB086 KB101 KB106 KB116 KB126 KB136 KB146 KB151 KB166 KB171 KB186 KB191 KB196 KM036 KM041 KM056 KM061 KM066 KM081 KM086 KM101 KM106 KM116 KM126 KM136 KM146 KM151 KM166 KM171 KM186 KM191 KM196 KU221 LB011 LB016 LB036 LB041 LB056 LB061 LB066 LB081 LB086 LB101 LB106 LB116 LB126 LB136 LB146 LB151 LB166 LB171 LB186 LB191 LB196 LE221 LG021 LG026 LG031 LG036 LG041 LG046 LG051 LG056 LG061 LG066 LG081 LG086 LG101 LG106 LG116 LG126 LG136 LG146 LG151 LG166 LG171 LG186 LG191 LG196 LJ201 LJ216 LJ221 LJ226 LJ231 LU046 LU051 LU056 LU061 LU066 LU081 LU086 LU101 LU106 LU116 LU126 LU136 LU146 LU151 LU166 LU171 LU186 LU191 LU196 ME021 ME046 ME051 ME056 ME061 ME066 ME071 ME076 ME081 ME086 ME091 ME096 ME101 ME106 ME111 ME116 ME121 ME126 ME131 ME136 ME141 ME146 ME151 ME156 ME161 ME166 ME171 ME176 ME181 ME186 ME191 ME196 ME221 MN021 MN051 MN056 MN076 MN081 MN086 MN101 MN116 MN121 MN126 MN141 MN156 MN161 MN166 MN186 MN191 MN221 NA021 NA026 NA051 NA056 NA186 NA191 NA216 NA221 NE051 NE056 NE186 NE191 NU026 NU051 NU056 NU081 NU121 NU161 NU186 NU191 NU216 PA026 PA051 PA056 PA066 PA076 PA081 PA086 PA096 PA106 PA116 PA121 PA126 PA136 PA146 PA156 PA161 PA166 PA176 PA186 PA191 PA216 PJ026 PJ051 PJ081 PJ121 PJ161 PJ191 PJ216 RA026 RA051 RA056 RA186 RA191 RA216 RE026 RE051 RE191 RE216
VDDR	AA021 AA046 AA196 AA221 AE021 AE046 AE061 AE076 AE086 AE101 AE116 AE126 AE141 AE156 AE166 AE181 AE196 AE221 AJ001 AJ021 AJ046 AJ061 AJ076 AJ086 AJ101 AJ116 AJ126 AJ141 AJ156 AJ166 AJ181 AJ196 AJ221 AJ241 BA001 BA021 BA046 BA061 BA076 BA086 BA101 BA116 BA126 BA141 BA156 BA166 BA181 BA196 BA221 BA241 BJ001 BJ021 BJ046 BJ061 BJ071 BJ101 BJ111 BJ141 BJ171 BJ181 BJ196 BJ221 BJ241 BN001 BN021 BN046 BN061 BN076 BN086 BN101 BN116 BN126 BN141 BN156 BN166 BN181 BN196 BN221 BN241 CE001 CE021 CE026 CE046 CE061 CE076 CE086 CE101 CE116 CE126 CE141 CE156 CE166 CE181 CE196 CE216 CE221 CE241 CJ006 CJ031 CJ036 CJ041 CJ046 CJ061 CJ076 CJ086 CJ101 CJ116 CJ126 CJ141 CJ156 CJ166 CJ181 CJ196 CJ201 CJ206 CJ211 CJ231 CJ236 CJ241 CU001 CU016 CU026 CU041 CU046 CU061 CU066 CU071 CU091 CU096 CU106 CU111 CU131 CU136 CU146 CU151 CU171 CU176 CU181 CU196 CU201 CU216 CU226 CU241 DE001 DE016 DE026 DE041 DE201 DE216 DE226 DE241 DN001 DN016 DN026 DN041 DN201 DN216 DN226 DN241 EA206 EA211 EE201 EE216 EE226 EE241 EN201 EN216 EN226 EN241 FA201 FA216 FA226 FA241 FJ206 FJ211 FN201 FN216 FN226 FN241 GA201 GA216 GA226 GA241 GJ201 GJ216 GJ226 GJ241 JA201 JA216 JA226 JA241 JJ201 JJ216 JJ226 JJ241 JU201 JU216 JU226 JU241 KA206 KA211 KJ201 KJ216 KJ226 KJ241 KU201 KU216 KU226 KU241 LE201 LE216 LE226 LE241 LJ206 LJ211 LU001 LU016 LU026 LU041 LU201 LU216 LU226 LU241 ME001 ME016 ME026 ME041 ME201 ME216 ME226 ME241 MN001 MN016 MN026 MN041 MN046 MN061 MN066 MN071 MN091 MN096 MN106 MN111 MN131 MN136 MN146 MN151 MN171 MN176 MN181 MN196 MN201 MN216 MN226 MN241 NA006 NA031 NA036 NA041 NA046 NA061 NA076 NA086 NA101 NA116 NA126 NA141 NA156 NA166 NA181 NA196 NA201 NA206 NA211 NA231 NA236 NA241 NE001 NE021 NE026 NE046 NE061 NE076 NE086 NE101 NE116 NE126 NE141 NE156 NE166 NE181 NE196 NE216 NE221 NE241 NU001 NU021 NU046 NU061 NU076 NU086 NU101 NU116 NU126 NU141 NU156 NU166 NU181 NU196 NU221 NU241 PA001 PA021 PA046 PA061 PA071 PA101 PA111 PA141 PA171 PA181 PA196 PA221 PA241 PJ001 PJ021 PJ046 PJ061 PJ076 PJ086 PJ101 PJ116 PJ126 PJ141 PJ156 PJ166 PJ181 PJ196 PJ221 PJ241 RA001 RA021 RA046 RA061 RA076 RA086 RA101 RA116 RA126 RA141 RA156 RA166 RA181 RA196 RA221 RA241 RE021 RE046 RE061 RE076 RE086 RE101 RE116 RE126 RE141 RE156 RE166 RE181 RE196 RE221 RJ021 RJ046 RJ196 RJ221

Table 4-2. Power Rails (Page 3 of 4)

Rail	BGA List
GND	AA011 AA016 AA026 AA031 AA036 AA041 AA051 AA061 AA076 AA081 AA086 AA101 AA116 AA121 AA126 AA141 AA156 AA161 AA166 AA181 AA191 AA201 AA206 AA211 AA216 AA226 AA231 AN001 AN006 AN011 AN016 AN021 AN026 AN031 AN036 AN041 AN046 AN051 AN056 AN061 AN076 AN081 AN086 AN101 AN116 AN121 AN126 AN141 AN156 AN161 AN166 AN181 AN186 AN191 AN196 AN201 AN206 AN211 AN216 AN221 AN226 AN231 AN236 AN241 AU001 AU021 AU026 AU046 AU051 AU061 AU076 AU081 AU086 AU101 AU116 AU121 AU126 AU141 AU156 AU161 AU166 AU181 AU191 AU196 AU216 AU221 AU241 BE001 BE011 BE036 BE046 BE051 BE056 BE061 BE066 BE071 BE081 BE091 BE096 BE101 BE106 BE111 BE121 BE131 BE136 BE141 BE146 BE151 BE161 BE171 BE176 BE181 BE186 BE191 BE196 BE206 BE231 BE241 BU001 BU006 BU011 BU016 BU021 BU026 BU031 BU036 BU041 BU046 BU051 BU056 BU061 BU076 BU081 BU086 BU101 BU116 BU121 BU126 BU141 BU156 BU161 BU166 BU181 BU186 BU191 BU196 BU201 BU206 BU211 BU216 BU221 BU226 BU231 BU236 BU241 CA001 CA021 CA026 CA046 CA051 CA056 CA061 CA076 CA081 CA086 CA101 CA116 CA121 CA126 CA141 CA156 CA161 CA166 CA181 CA186 CA191 CA196 CA216 CA221 CA241 CN016 CN021 CN026 CN031 CN036 CN041 CN046 CN051 CN056 CN061 CN076 CN081 CN086 CN101 CN116 CN121 CN126 CN141 CN156 CN161 CN166 CN181 CN186 CN191 CN196 CN201 CN206 CN211 CN216 CN221 CN226 DA001 DA016 DA021 DA026 DA041 DA046 DA051 DA056 DA061 DA066 DA071 DA076 DA081 DA086 DA091 DA096 DA101 DA106 DA111 DA116 DA121 DA126 DA131 DA136 DA141 DA151 DA156 DA161 DA166 DA171 DA176 DA181 DA186 DA191 DA196 DA201 DA216 DA221 DA226 DA241 DJ001 DJ016 DJ026 DJ041 DJ046 DJ051 DJ056 DJ061 DJ066 DJ071 DJ076 DJ081 DJ086 DJ091 DJ101 DJ106 DJ111 DJ116 DJ121 DJ126 DJ131 DJ136 DJ141 DJ146 DJ151 DJ156 DJ161 DJ166 DJ171 DJ176 DJ181 DJ186 DJ191 DJ196 DJ201 DJ216 DJ226 DJ241 DU001 DU016 DU021 DU026 DU041 DU046 DU051 DU056 DU061 DU066 DU071 DU076 DU081 DU086 DU091 DU096 DU101 DU106 DU111 DU116 DU121 DU126 DU131 DU136 DU141 DU146 DU151 DU156 DU161 DU166 DU171 DU176 DU181 DU186 DU191 DU196 DU201 DU216 DU221 DU226 DU241 EG001 EG006 EG011 EG016 EG021 EG026 EG031 EG036 EG041 EG046 EG056 EG061 EG066 EG071 EG076 EG081 EG086 EG091 EG096 EG101 EG106 EG111 EG116 EG121 EG126 EG131 EG136 EG141 EG146 EG151 EG156 EG161 EG166 EG171 EG176 EG181 EG186 EG191 EG196 EJ201 EJ216 EJ221 EJ226 EJ241 EM001 EM006 EM011 EM016 EM021 EM026 EM031 EM036 EM041 EM046 EM051 EM056 EM061 EM066 EM071 EM076 EM081 EM086 EM091 EM096 EM101 EM106 EM111 EM116 EM121 EM126 EM131
GND	EM136 EM141 EM146 EM151 EM156 EM161 EM166 EM171 EM176 EM181 EM186 EM191 EM196 EU201 EU216 EU226 EU241 FB051 FB056 FB061 FB066 FB071 FB076 FB081 FB086 FB091 FB096 FB101 FB106 FB111 FB116 FB121 FB126 FB131 FB136 FB141 FB146 FB151 FB156 FB161 FB166 FB171 FB176 FB181 FB186 FB191 FB196 FE201 FE216 FE221 FE226 FE241 FM001 FM006 FM011 FM016 FM021 FM026 FM031 FM036 FM046 FM051 FM056 FM061 FM066 FM071 FM076 FM081 FM086 FM091 FM096 FM101 FM106 FM111 FM116 FM121 FM126 FM131 FM136 FM141 FM146 FM151 FM156 FM161 FM166 FM171 FM176 FM181 FM186 FM191 FM196 FU201 FU216 FU221 FU226 FU241 GB051 GB066 GB071 GB081 GB086 GB091 GB096 GB101 GB106 GB111 GB116 GB121 GB126 GB131 GB136 GB141 GB146 GB151 GB156 GB161 GB166 GB171 GB176 GB181 GB186 GB191 GB196 GE201 GE216 GE226 GE241 GM001 GM006 GM011 GM016 GM021 GM026 GM031 GM036 GM041 GM046 GM066 GM071 GM076 GM081 GM086 GM091 GM096 GM101 GM106 GM111 GM116 GM121 GM126 GM131 GM136 GM141 GM146 GM151 GM156 GM161 GM166 GM171 GM176 GM181 GM186 GM191 GM196 GN201 GN216 GN221 GN226 GN241 GU221 GU231 HB051 HB056 HB061 HB066 HB071 HB076 HB081 HB086 HB091 HB096 HB101 HB106 HB111 HB116 HB121 HB126 HB131 HB136 HB141 HB146 HB151 HB156 HB161 HB166 HB171 HB176 HB181 HB186 HB191 HB196 HE201 HE211 HE221 HE231 HE241 HM051 HM056 HM061 HM066 HM071 HM076 HM081 HM086 HM091 HM096 HM101 HM106 HM111 HM116 HM121 HM126 HM131 HM136 HM141 HM146 HM151 HM156 HM161 HM166 HM171 HM176 HM181 HM186 HM191 HM196 HN221 HN231 HU201 HU216 HU221 HU226 HU241 JB006 JB011 JB016 JB021 JB026 JB031 JB036 JB041 JB046 JB051 JB056 JB061 JB066 JB071 JB076 JB081 JB086 JB091 JB096 JB101 JB106 JB111 JB116 JB121 JB126 JB131 JB136 JB141 JB146 JB151 JB156 JB161 JB166 JB171 JB176 JB181 JB186 JB191 JB196 JE201 JE216 JE226 JE241 JM051 JM056 JM061 JM066 JM071 JM076 JM081 JM086 JM091 JM096 JM101 JM106 JM111 JM116 JM121 JM126 JM131 JM136 JM141 JM146 JM151 JM156 JM161 JM166 JM171 JM176 JM181 JM186 JM191 JM196 JN201 JN216 JN221 JN226 JN241 KE201 KE216 KE221 KE226 KE241 KG001 KG006 KG021 KG026 KG031 KG036 KG041 KG046 KG051 KG056 KG061 KG066 KG071 KG076 KG081 KG086 KG091 KG096 KG101 KG106 KG111 KG116 KG121 KG126 KG131 KG136 KG141 KG146 KG151 KG156 KG161 KG166 KG171 KG176 KG181 KG186 KG191 KG196 KN201 KN216 KN226 KN241 KU011 KU021 KU026 KU031 KU036 KU046 KU051 KU056 KU061 KU066 KU071 KU076 KU081 KU086 KU091 KU096 KU101 KU106 KU111 KU116 KU121 KU126 KU131 KU136 KU141 KU146 KU151 KU156 KU161 KU166 KU171 KU176 KU181

Table 4-2. Power Rails (Page 4 of 4)

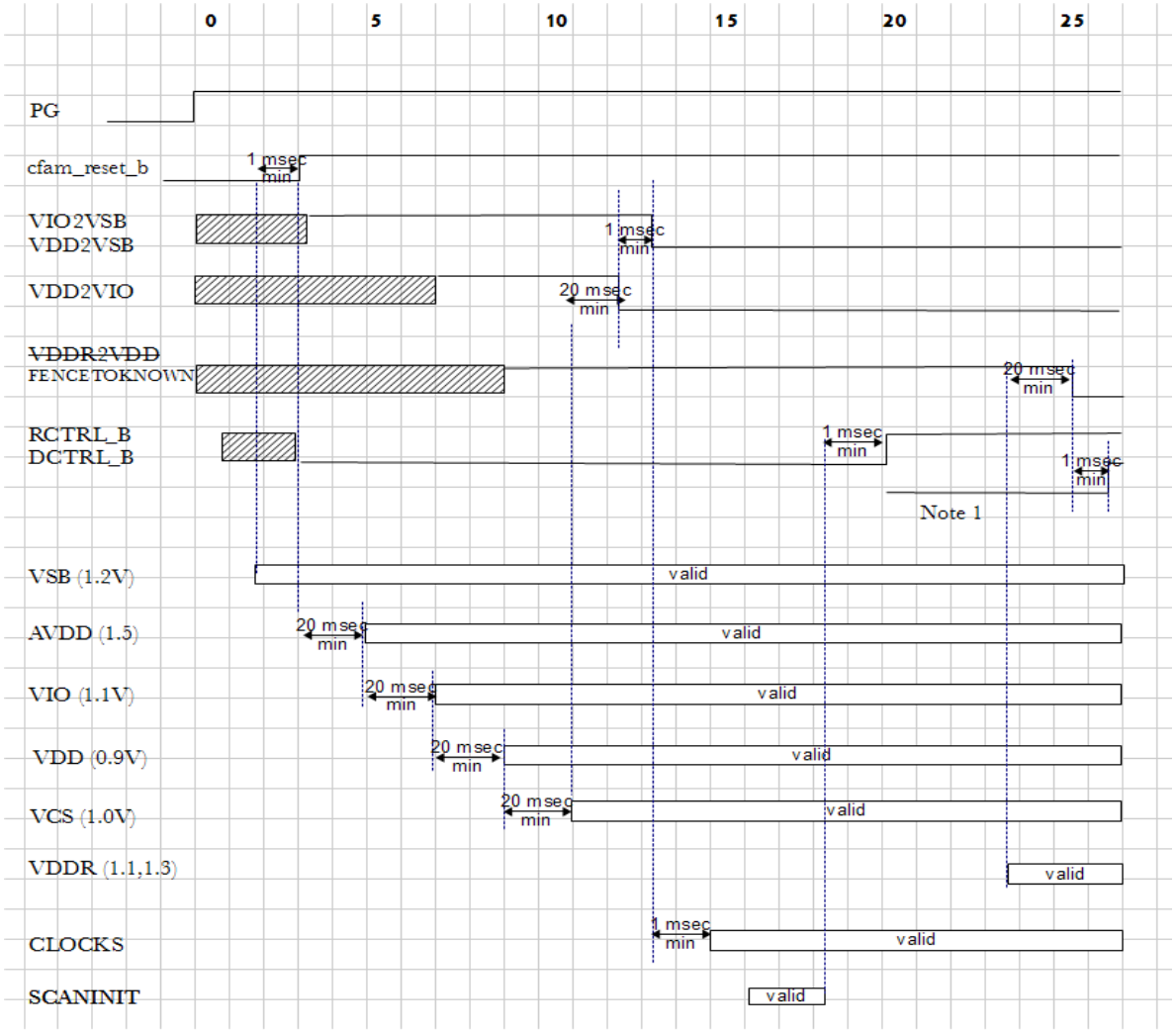
Rail	BGA List
GND	KU186 KU191 KU196 LA201 LA216 LA221 LA226 LA241 LN001 LN016 LN021 LN026 LN041 LN046 LN051 LN056 LN061 LN066 LN071 LN076 LN081 LN086 LN091 LN096 LN101 LN106 LN111 LN116 LN121 LN126 LN131 LN136 LN141 LN146 LN151 LN156 LN161 LN166 LN171 LN176 LN181 LN186 LN191 LN196 LN201 LN216 LN221 LN226 LN241 MA001 MA016 MA026 MA041 MA046 MA051 MA056 MA061 MA066 MA071 MA076 MA081 MA086 MA091 MA101 MA106 MA111 MA116 MA121 MA126 MA131 MA136 MA141 MA146 MA151 MA156 MA161 MA166 MA171 MA176 MA181 MA186 MA191 MA196 MA201 MA216 MA226 MA241 MJ001 MJ016 MJ021 MJ026 MJ041 MJ046 MJ051 MJ056 MJ061 MJ066 MJ071 MJ076 MJ081 MJ086 MJ091 MJ096 MJ101 MJ106 MJ111 MJ116 MJ121 MJ126 MJ131 MJ136 MJ141 MJ146 MJ151 MJ156 MJ161 MJ166 MJ171 MJ176 MJ181 MJ186 MJ191 MJ196 MJ201 MJ216 MJ221 MJ226 MJ241 MU016 MU021 MU026 MU031 MU036 MU041 MU046 MU051 MU056 MU061 MU076 MU081 MU086 MU101 MU116 MU121 MU126 MU141 MU156 MU161 MU166 MU181 MU186 MU191 MU196 MU201 MU206 MU211 MU216 MU221 MU226 NJ001 NJ021 NJ026 NJ046 NJ051 NJ056 NJ061 NJ076 NJ081 NJ086 NJ101 NJ116 NJ121 NJ126 NJ141 NJ156 NJ161 NJ166 NJ181 NJ186 NJ191 NJ196 NJ216 NJ221 NJ241 NN001 NN006 NN011 NN016 NN021 NN026 NN031 NN036 NN041 NN046 NN051 NN056 NN061 NN076 NN081 NN086 NN101 NN116 NN121 NN126 NN141 NN156 NN161 NN166 NN181 NN186 NN191 NN196 NN201 NN206 NN211 NN216 NN221 NN226 NN231 NN236 NN241 PE001 PE011 PE036 PE046 PE051 PE056 PE061 PE066 PE071 PE081 PE091 PE096 PE101 PE106 PE111 PE121 PE131 PE136 PE141 PE146 PE151 PE161 PE171 PE176 PE181 PE186 PE191 PE196 PE206 PE231 PE241 PN001 PN021 PN026 PN046 PN051 PN061 PN076 PN081 PN086 PN101 PN116 PN121 PN126 PN141 PN156 PN161 PN166 PN181 PN191 PN196 PN216 PN221 PN241 PU001 PU006 PU011 PU016 PU021 PU026 PU031 PU036 PU041 PU046 PU051 PU056 PU061 PU076 PU081 PU086 PU101 PU116 PU121 PU126 PU141 PU156 PU161 PU166 PU181 PU186 PU191 PU196 PU201 PU206 PU211 PU216 PU221 PU226 PU231 PU236 PU241 RJ011 RJ016 RJ026 RJ031 RJ036 RJ041 RJ051 RJ061 RJ076 RJ081 RJ086 RJ101 RJ116 RJ121 RJ126 RJ141 RJ156 RJ161 RJ166 RJ181 RJ191 RJ201 RJ206 RJ211 RJ216 RJ226 RJ231

5. Clocking and Test Functions

5.1 Power Sequencing

Figure 5-1 shows the required initialization power sequencing of the POWER8 Memory Buffer.

Figure 5-1. POWER8 Memory Buffer Power Sequence



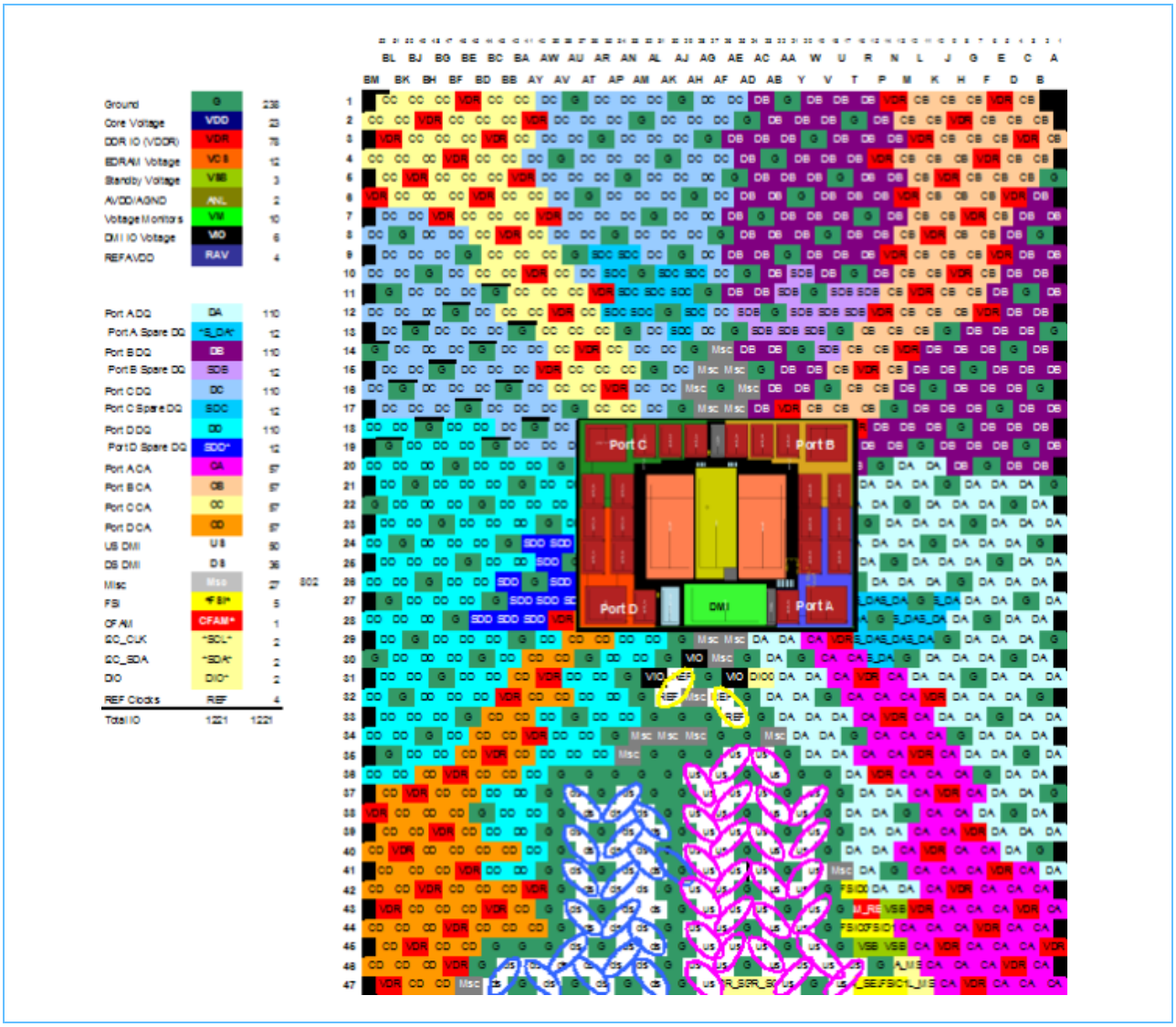
Note: The “RCTRL” and “DCTRL” for the transceivers on the VDDR domain are turned on via SCOM-microcode after the VDDR plane is enabled. At the time RCTRL and DCTRL are enabled, the SCOM registers must be initialized such that the VDDR transceivers are disabled.

6. POWER8 Memory Buffer Packaging and Physical Design

6.1 POWER8 Memory Buffer 4-Port Chip Package

The package size is 27.5 x 42.0 mm with 1.0 mm interstitial ball grid array pattern and a total of 1221 I/Os. The memory buffer chip is shown rotated 90 degrees in the package with the differential memory interface (DMI) facing south.

Figure 6-1. Memory Buffer 4-Port Package with Memory Buffer Chip Rotated 90 degrees



Note: This image is depicted from the C4 balls down in a “live bug” view.

6.1.1 Decoupling Capacitance Requirements

To meet the required noise margins, decoupling caps must be employed at several levels of the package hierarchy. *Table 6-1* shows the requirements at each level. There are two sets of on-die capacitance targets for most of the rails shown, indicating with and without embedded capacitors in the package. The without value represents the total on-die capacitance required to eliminate the embedded capacitor in the package.

The modeling includes on-die capacitance, capacitors embedded in the package (with 0201 size packages), and board-level capacitors. The Simplified term in the table represents preliminary modeling without the package mcm file. The noise margin modeling will be updated when the mcm file is available. The present modeling results represent on-die capacitance and board-level capacitance targets.

Figure 6-2. Memory Buffer Packaging Hierarchy with Embedded Capacitors

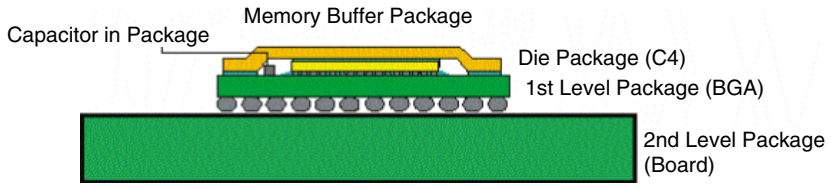


Table 6-1 table reflects the latest modeling with the package mcm file. The VIO step current input was reduced from 1.3 A to 0.5 A.

Table 6-1. Memory Buffer 4-Port Noise Margin Table with Capacitance Per Voltage Supply

Voltage Rail	Die Cap	Mod Cap	Brd Cap	Target	Post PD1[1]	Post PD2[1]
				mVpp	mVpp	mVpp
VDD	2.3 uf	2.2uf (1)	2.2 uf (20)	+/-45	+/-23.5	+/-29
VCS	300 nf	0	2.2 uf (5)	+/-51	+/-20.5	+/-19.5
VIO[2]	500 nf	0	47 uf (4)	+/-55	+/-18	+/-16
VDDR	200 nf	0	47 uf + (30)	+/-25	+/-3.5	+/-5

1. Post PD1 represents modeling the memory buffer laminate prior to completion, and Post PD2 represents the finished laminate.
2. The VIO noise margin table was updated with on-die and on-DIMM capacitance values, yielding the same results.

6.2 DDR I/O Specification

6.2.1 DDR Output Driver Impedance (R_{ON})

The driver impedance is programmable by a configuration register in the DDR unit to one of the allowable nominal values shown in *Table 6-2*. These impedances have a tolerance of ±14%.

Table 6-2. Driver Impedance

DDR Facility	DDR PHY	Configurable	Supported Impedance Settings (Ω)		
			Minimum	Nominal	Maximum
M[ABCD]_DQ, M[ABCD]_DQS_[PN]	DP18	Per Port	20.64, 25.8, 29.5, 34.4	24, 30, 34.3, 40	27.36, 34.2, 39.10, 45.6
M[ABCD]_CMD_[A, BA, RASN, CASN, WEN PAR] M[ABCD][01[_CNTL_[CSN, CKE, ODT]	ADR52	Per I/O	12.9, 17.2, 25.8, 34.4	15, 20, 30, 40	17.1, 22.8, 39.10, 45.6
Note: M[ABCD}_RESETN does not use programmable drive impedance.					

6.2.2 DDR Receiver On-Die Termination

Termination values are based on a 240 Ω external calibration resistance. The ODT values are specified from VDDR/2 to ac ground using equal slice counts and resistance (R) for both the pull-up and pull-down sides of the driver as shown in *Figure 6-3*. The termination tolerance is ±14%.

Figure 6-3. ODT Termination Circuit

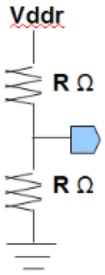


Table 6-3. Supported DDR Receiver On-Die Termination Settings

DDR Facility	DDR PHY	Configurable	Supported Termination Settings (Ω)			
			R	ODT Minimum	ODT Nominal	ODT Maximum
M[ABCD]_DQ, M[ABCD]_DQS_[PN]	DP18	Per Port	30, 40, 60, 80, 96, 120, 240	12.9, 17.2, 25.8, 34.4, 41.28 51.6, 103.2	15, 20, 30, 40, 48, 60, 120	17.1, 22.8, 34.2, 45.6, 54.72, 68.4, 136.8
Note: M[ABCD}_ERRN & M[ABCD]_EVENTN does not use programmable receiver termination.						

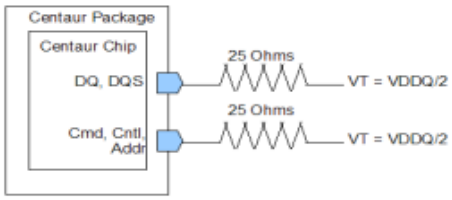
6.2.3 DDR Driver Slew Rates

Table 6-4. Supported DDR Driver Slew Rates

DDR Facility	DDR PHY	Configurable	Options	Supported Slew Rates			
				Slow Slew		Fast Slew	
				Mimum	Maximum	Mimum	Maximum
M[ABCD]_DQ	DP18	Per Port					
M[ABCD]_DQS_[PN]	DP18	Per Port	1.35 V 24 Ω	6	12	8	16
			1.35 V 30 Ω	6	12	8	16
			1.35 V 35 Ω	6	12	8	16
			1.35 V 40 Ω	6	12	8	16
M[ABCD]_CMD_[A, BA, RASN, CASN, WEN PAR] M[ABCD][01[_CNTL_[CSN, CKE, ODT]	ADR52	Per I/O	1.35 V 15 Ω	3	6	n/a	n/a
			1.35 V 20 Ω	3	6	n/a	n/a
			1.35 V 30 Ω	2	4	n/a	n/a
			1.35 V 40 Ω	2	4	n/a	n/a
Note: M[ABCD}_RESETN does not use programmable driver slew rates.							

The reference load specification shown in *Figure 6-4* should be used for slew rate modeling and hardware testing.

Figure 6-4. Slew Rate Reference Load Model



6.2.4 DDR VREF Driver Settings

There are two VREF drivers per memory port (M[ABCD]0_VREF and M[ABCD]1_VREF). This permits per socket control of the output reference voltage in situations where different vendor DIMMs are plugged into each socket. The supported ranges are:

- For DDR3, the supported range is 0.42 x DVDD through 0.575 x DVDD with 32 programmable step sizes of 0.5% of DVDD.
- For DDR4, no support is required because the DRAM has its own internal reference.

6.2.5 DDR DQ VREF Trimmer Control

Every DDR data byte (M[ABCD}_DQ) has independently programmable MCVREF inputs that support the following ranges through the use of configuration settings, providing an increment and decrement granularity of 1.375%. Although each nibble within a byte has separate circuits, they share a common setting.

- For DDR3, the supported range is from 0.5 x DVDD up to 0.61 x DVDD (+11%) and 0.5 x DVDD down to 0.4041 x DVDD (-9.59%)
- For DDR4, the supported range is from 0.7*DVDD up to 0.81*DVDD (+11%) and 0.7 x DVDD down to 0.6041 x DVDD (-9.59%)

6.3 Special Pin Requirements

- The M[ABCD]_CMD_ERRN and M[ABCD]_CMD_EVENTN pins require external 1 KΩ pull-up resistors on the card to ensure that these signals are logically inactive for topologies where they aren't driven, or during phases of the power-on reset (POR) sequence.
- The M[ABCD]_CMD_RESETN pin requires an external 1 KΩ pull-down resistor on the card to ensure that it is logically active until such time in the POR sequence that it can be actively controlled.
- The FAULT_N pin is a dotted bidirectional net that requires a system-level 1 KΩ pull-up resistor to ensure it remains logically inactive while all the drivers are in a high-impedance state. Use redundant pull-up resistors to increase reliability of this critical error reporting circuit.

Signal Name	Planar	
	Resistor	Supply
m[abcd]_cmd_resetn	1 KΩ Pull-down	GND
m[abcd]_errn	1 KΩ Pull-up[1]	1.35 V
m[abcd]_eventn	1 KΩ Pull-up	1.35 V
dio(0:1)	Not connected	Not connected
scl_mstr (rfu_vsb0)	1.2 KΩ Pull-up	3.3 V
sda_mstr (rfu_vsb1)	1.2 KΩ Pull-up	3.3 V
fault_n	1 KΩ Pull-up	0.9 V
fsi_sel_b	10 KΩ Pull-down	GND
fsid[01]	750 Ω Pull-up	1.2 V
pll_bypass	Not required	Not required
iot_card_test_bsc	Not required	Not required
ce0_te	No resistor	GND
cfam_reset_b	1 KΩ Pull-up	1.2 V

1. For DDR3 applications, the pull-up is required. For DDR4, the ERRN pin becomes the ALERTN to support DRAM parity checking and, therefore, is actively driven by the DRAMs in a dot-OR structure. The POWER8 Memory Buffer does not support this parity checking function.